

# COMPAL CONFIDENTIAL

MODEL NAME :EDC40

PCB NO : LA-G871P

BOM P/N : 431ADY31L0x

## Merion 14 AR

Whiskey lake-U U42

2019-03-05

REV : 1.0 (A00)

@ : Nopop Component

EMI@ : EMI Component

@EMI@ : EMI Nopop Component

ESD@ : ESDComponent

@ESD@ : ESD Nopop Component

RF@ : RF Component

@RF@ : RF Nopop Component

CONN@ : Connector Component

CXDP@ : XDP Component

DS3@ : Deep sleep support

NDS3@ : non Deep sleep support

750@ : NUVOTON NPCT750 TPM Component

ST33@ : ST33HTPH TPM Component

RTD3@ : RTD3 support

@RTD3@ : RTD3 Nopop Component

NRTD3@ : non RTD3 support

VPRO@ : vPro Component

NVPRO@ : Non-vPro Component

JUMP@ : Jump solder and short

@JUMP@ : Jump no solder

i7@ : Only i7 config support 4\*4 antenna

Power CKT : Merion 14\_WHL\_PWR\_X02\_1228a

GPIO map : 20181221a Rev1.5

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Cover Sheet

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1.0

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MB PCB

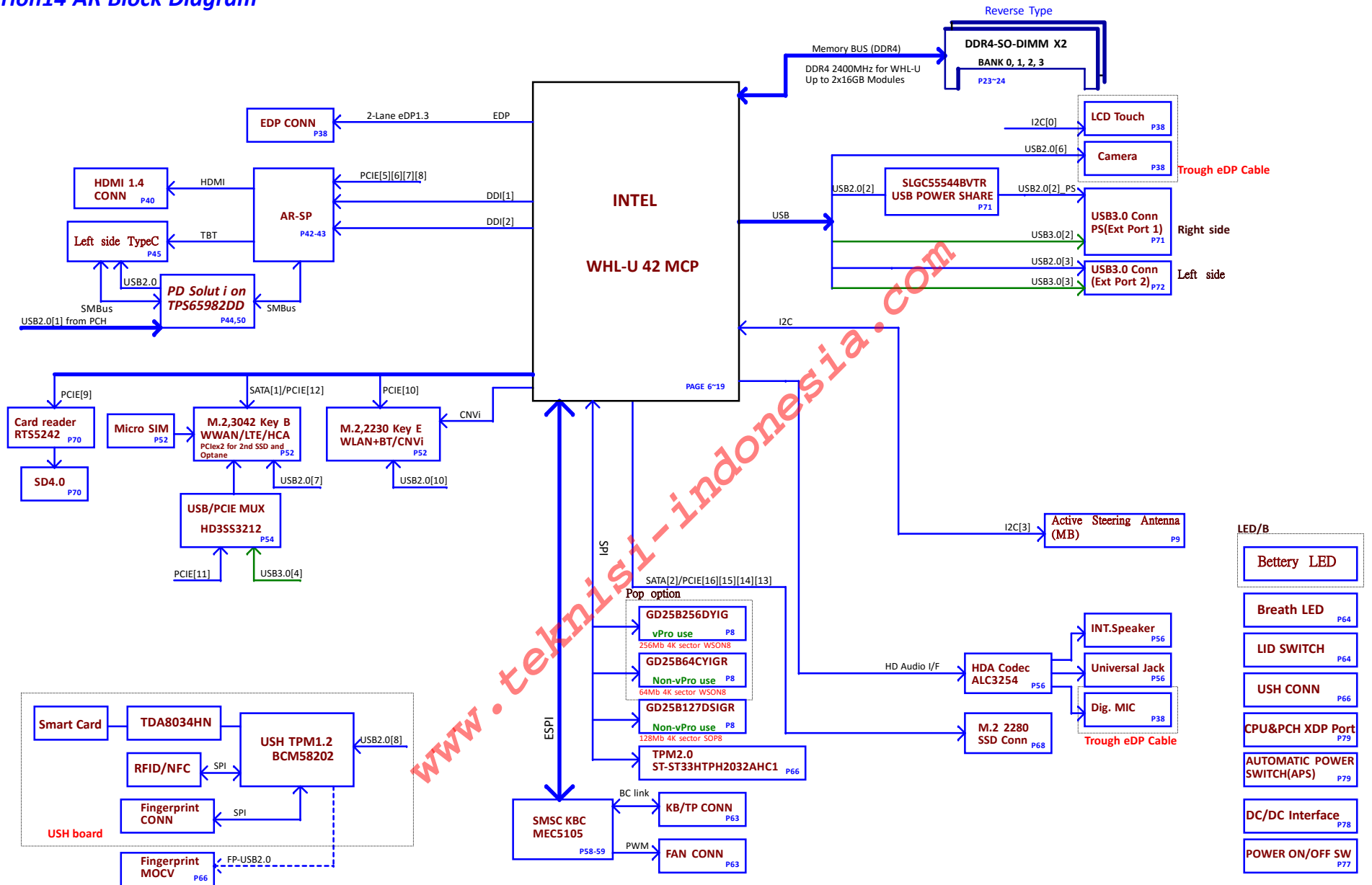
Part Number	Description
DAA000HW010	PCB 2EE LA-G871P REV1 MB AR 1

Layout Dell logo



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REV:A00  
PWB:7YM2P

# Merion14 AR Block Diagram



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Block Diagram			
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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1		PCIE-1		N/A
USB3.0-2		PCIE-2		JUSB1-->Right
USB3.0-3		PCIE-3		JUSB2-->Left
USB3.0-4		PCIE-4		M.2 3042(LTE)
USB3.0-5		PCIE-5		Alpine Ridge - SP
USB3.0-6		PCIE-6		
		PCIE-7		
		PCIE-8		
		PCIE-9		Card Reader
		PCIE-10		M.2 2230(WLAN)
		PCIE-11	SATA-0	M.2 3042(LTE)
		PCIE-12	SATA-1	
		PCIE-13		M.2 2280 SSD (PCIex4 or SATA)
		PCIE-14		
		PCIE-15	SATA-1*	
		PCIE-16	SATA-2	

USB PORT#	DESTINATION
1	Type C
2	JUSB1-->Right
3	JUSB2-->Left
4	N/A
5	N/A
6	Camera
7	M2 3042(WWAN)
8	USH
9	Reserve for FPR in PB
10	M.2 2230(BT)

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_PRIM	+1.2V_MEM +2.5V_MEM +1.0V_VCCSTG	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN
S0	ON	ON	ON
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	GbE	GbE	GbE		SATA 0	SATA 1a	GbE	GbE	SATA 1b	SATA 2
Intel® RST Support	No Support				No Support				Yes				Yes			

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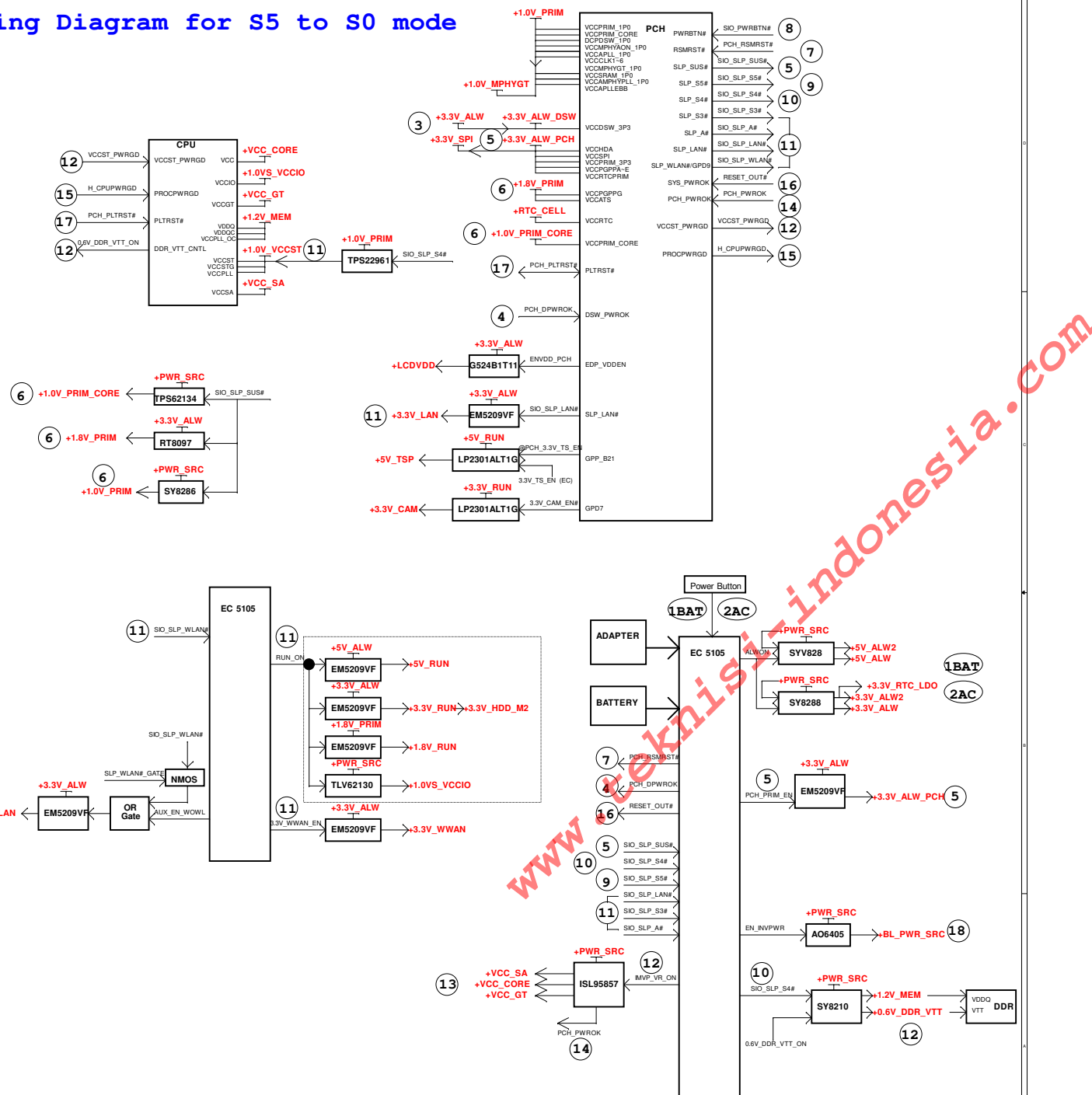


Title		Port assignment	
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### Timing Diagram for S5 to S0 mode



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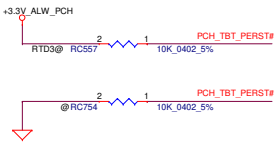
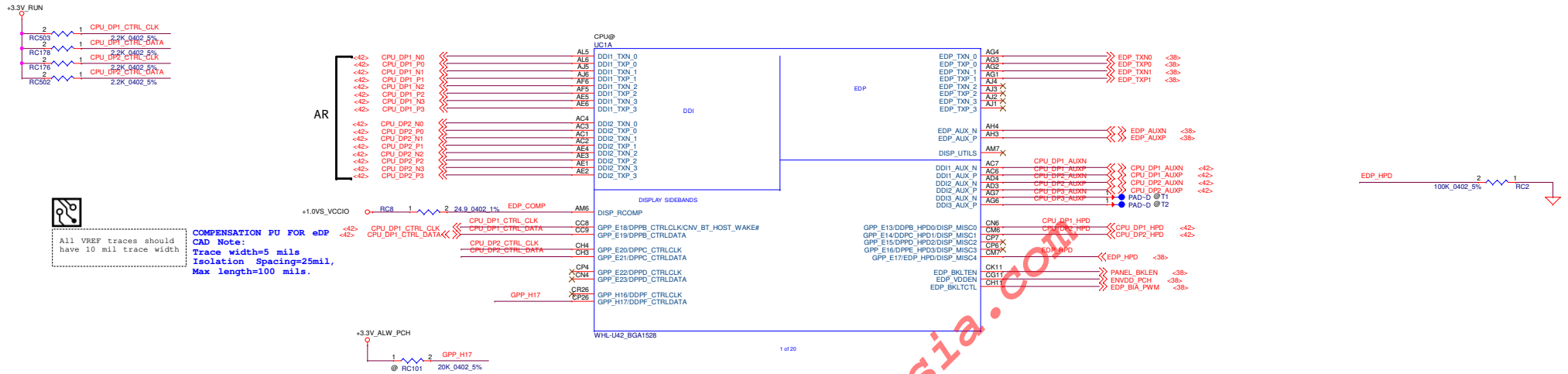
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### Power Sequence

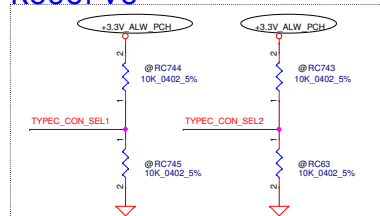
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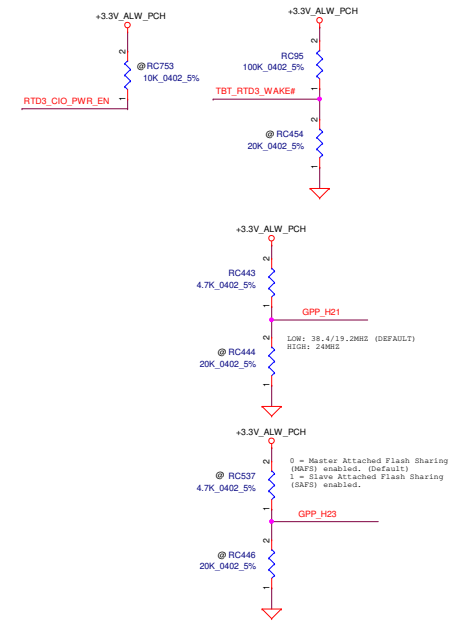
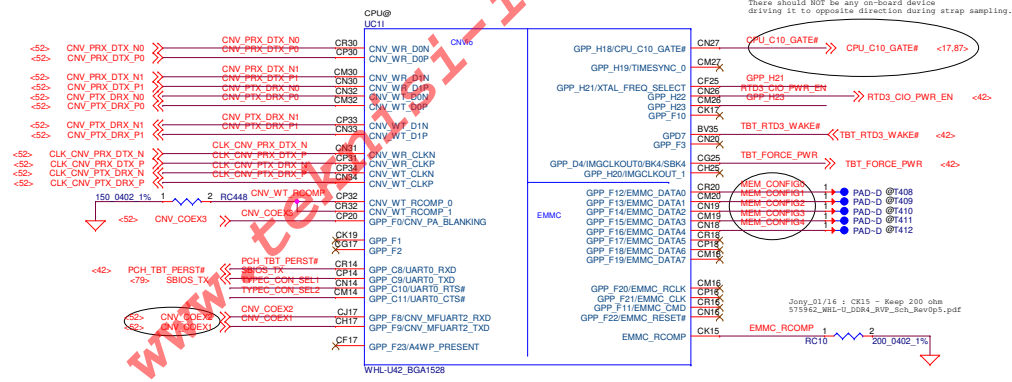
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## Reserve



Vendor	JAE	FOXCON	TBD	TBD
TYPE_CON_SEL1	LOW	LOW	HIGH	HIGH
TYPE_CON_SEL2	LOW	HIGH	LOW	HIGH



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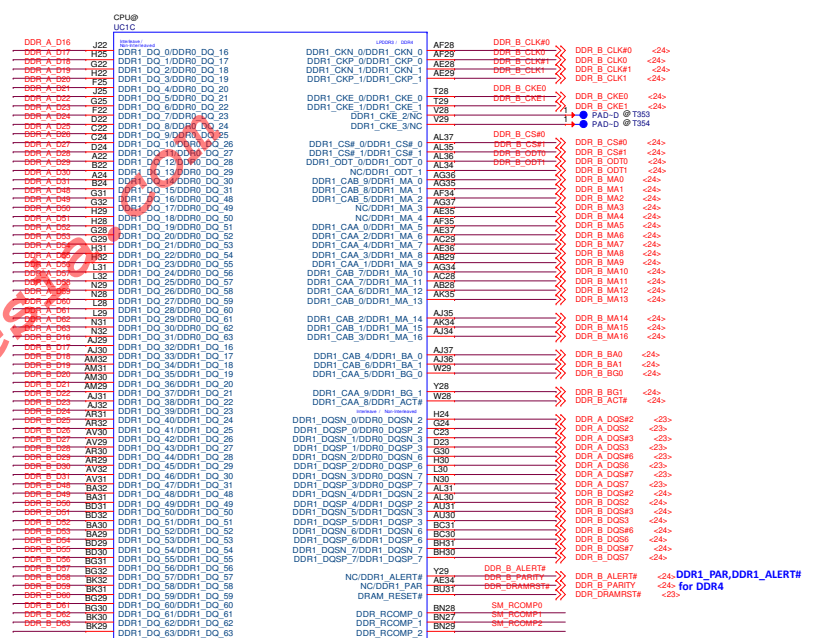
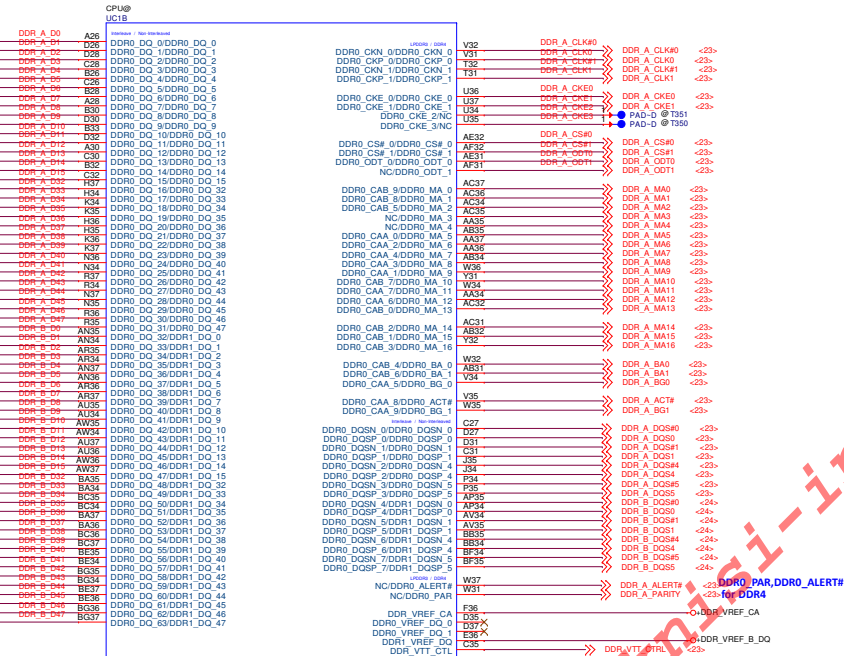
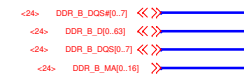
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CPU(1/14)DDI,EDP,CS12,EMMC

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### DDR4, Ballout for side by side(Non-Interleave)



**CAD Note:**  
Trace width=12~15 mil, Spacing=20 mils  
Max trace length= 500 mil

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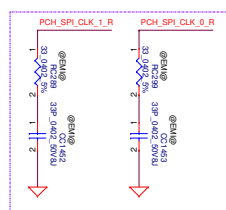
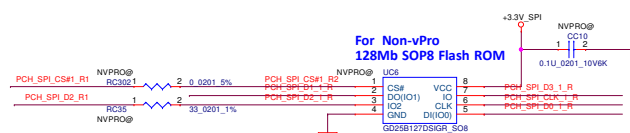
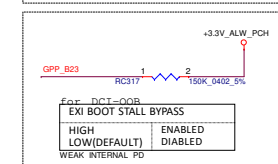
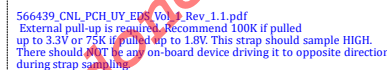
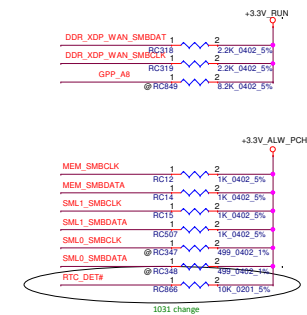
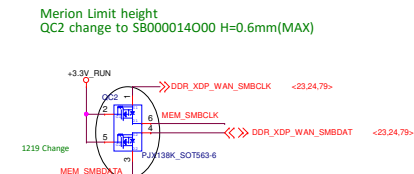
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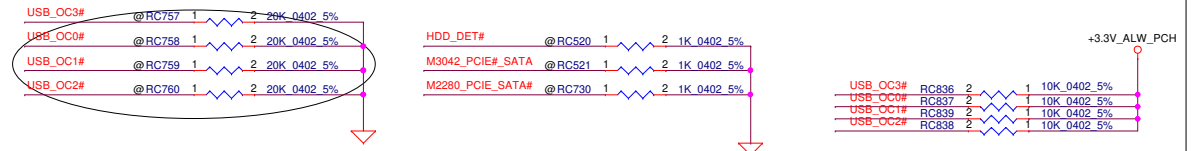
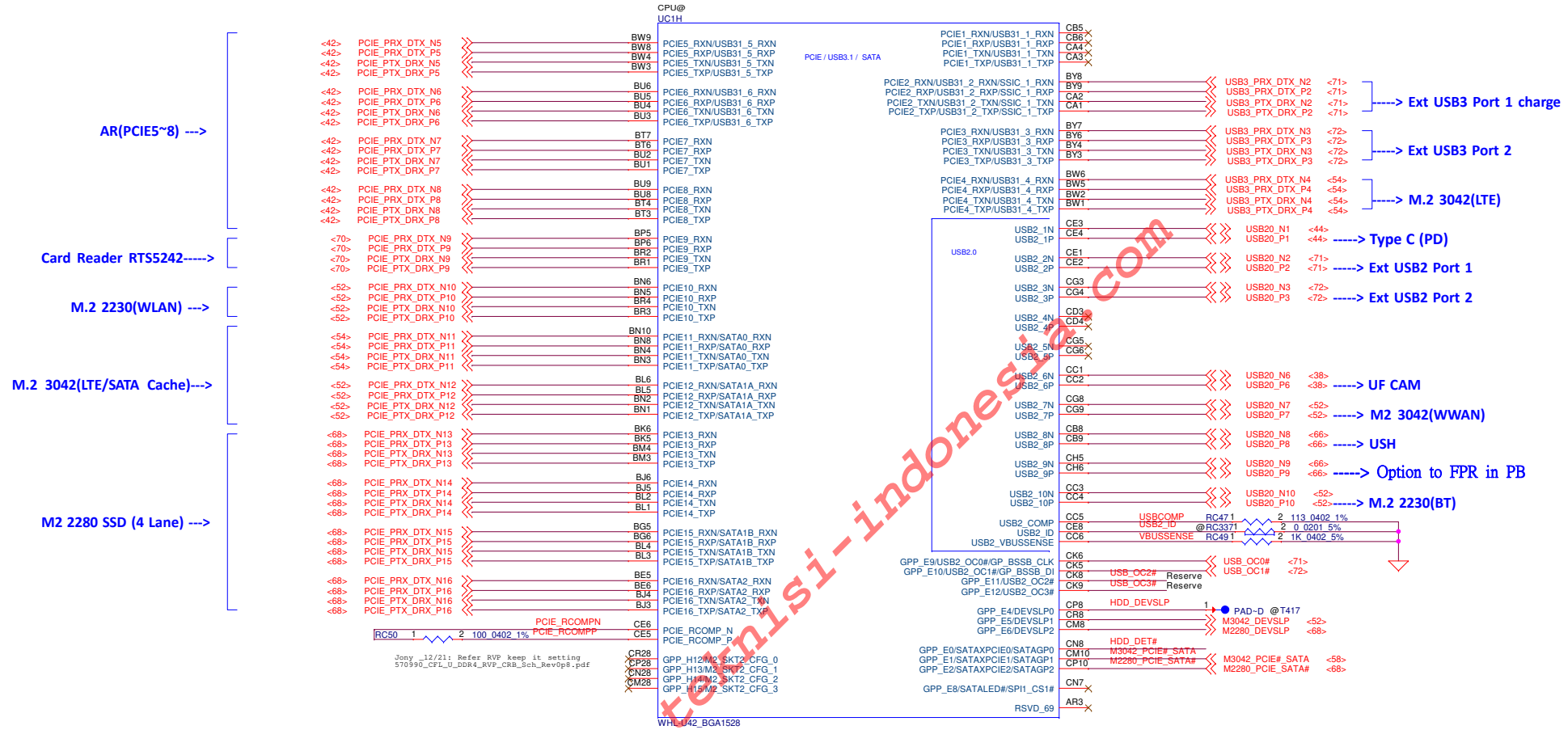


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# For Merion AR (follow WHL 180416a port map)



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Title			
CPU(5/14)PCIE,USB,SATA			
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M.2 3042 WWAN→

M.2 2230 WLAN→

M.2 2280 SSD→

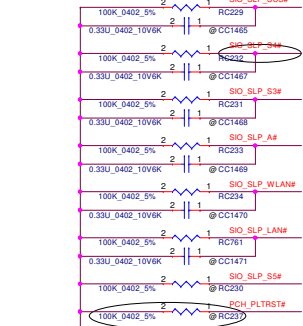
Card Reader→

AR→

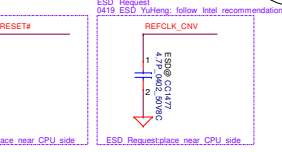
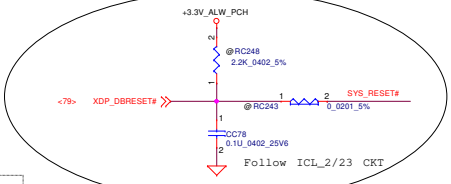
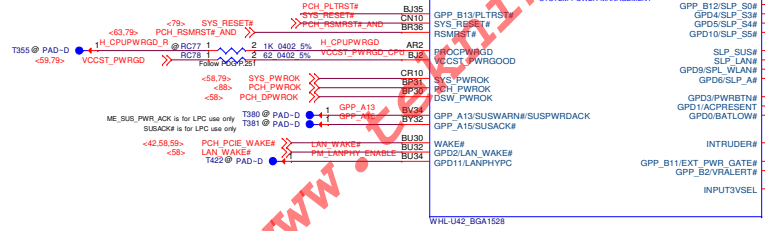
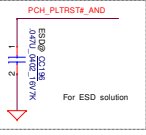
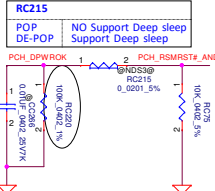
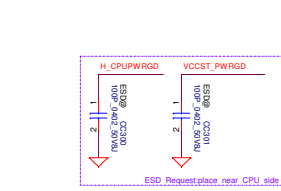
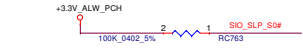
+3.3V\_ALW\_DSW

+1.0V\_VCCST

PCH GLITCH ISSUE MITIGATION(PDG p.130)

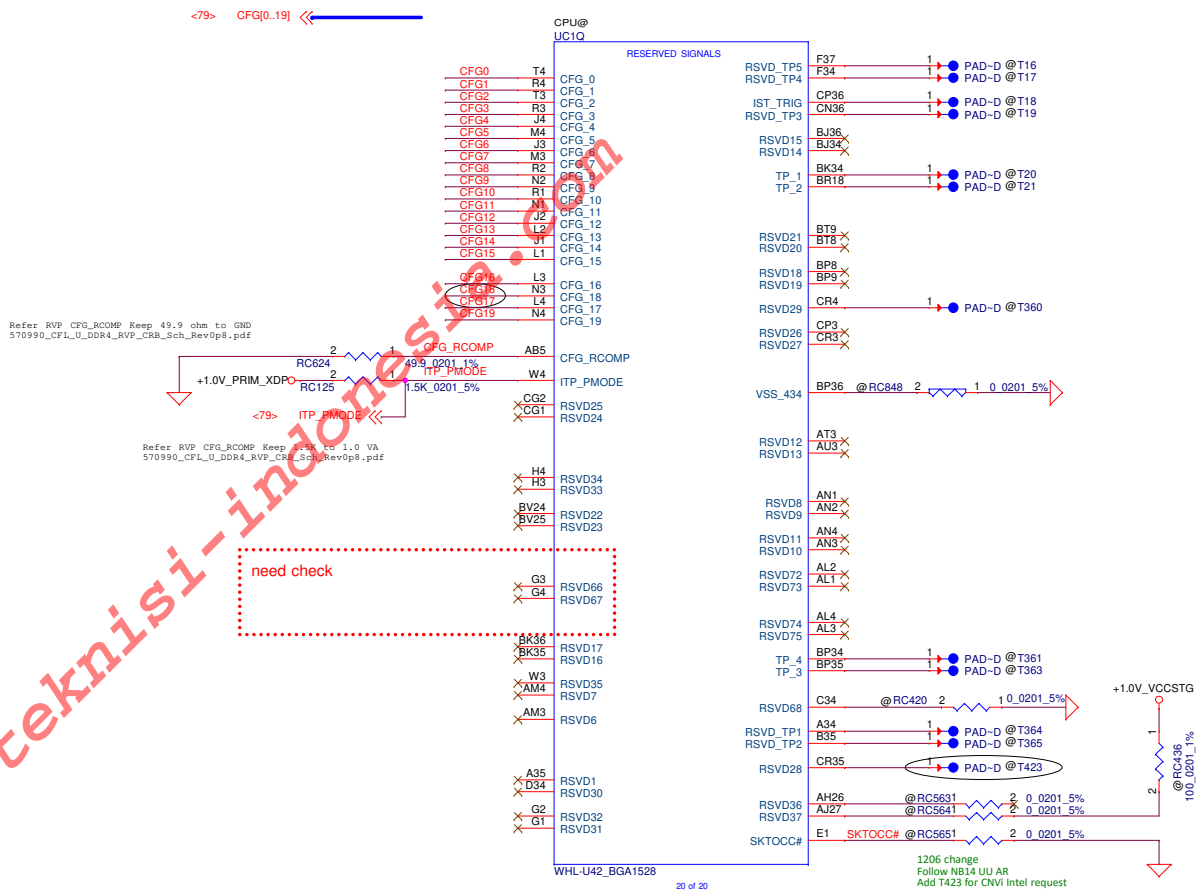
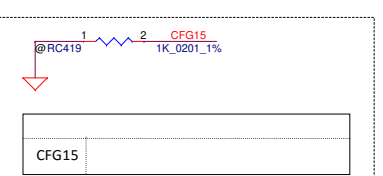
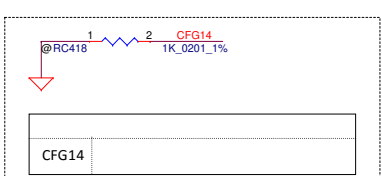
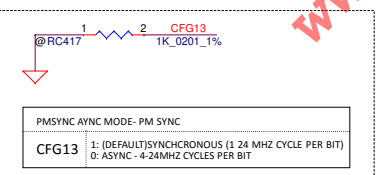
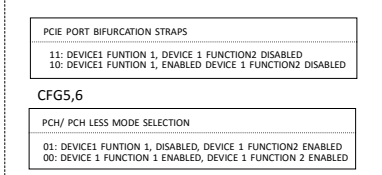
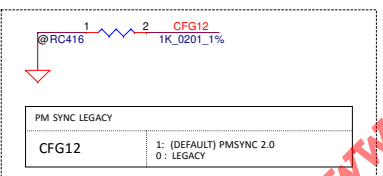
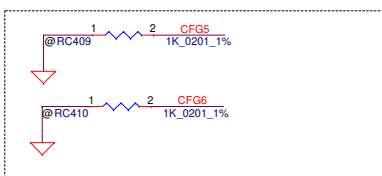
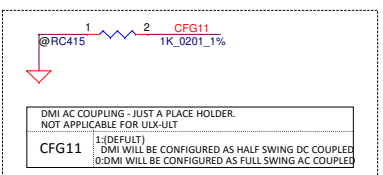
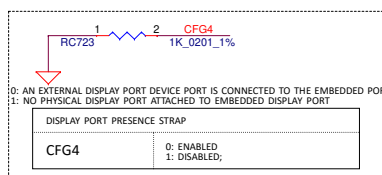
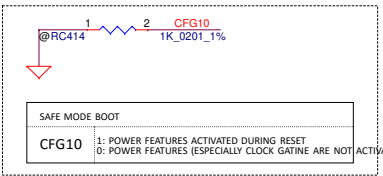
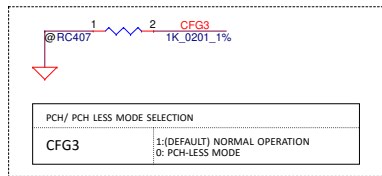
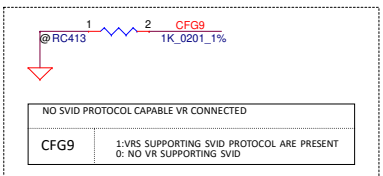
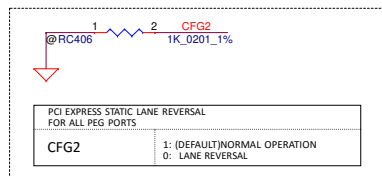
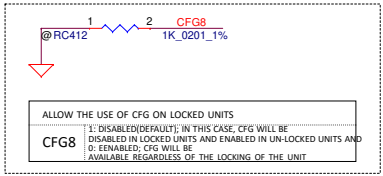
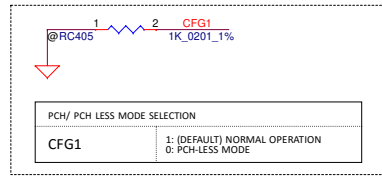
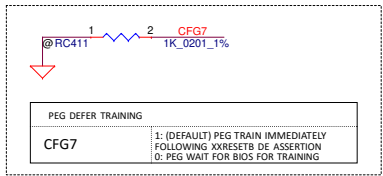
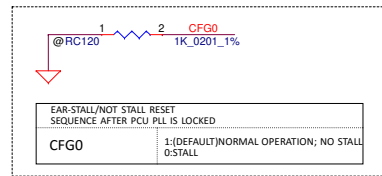


T211 change  
Follow NB14 UU AR, Intel CNV1 recommendation RC237 pop.  
But measure cold reset and Global reset sequence timing fail, So depop RC237



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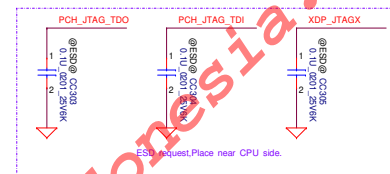
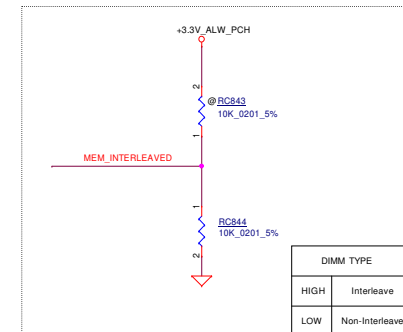
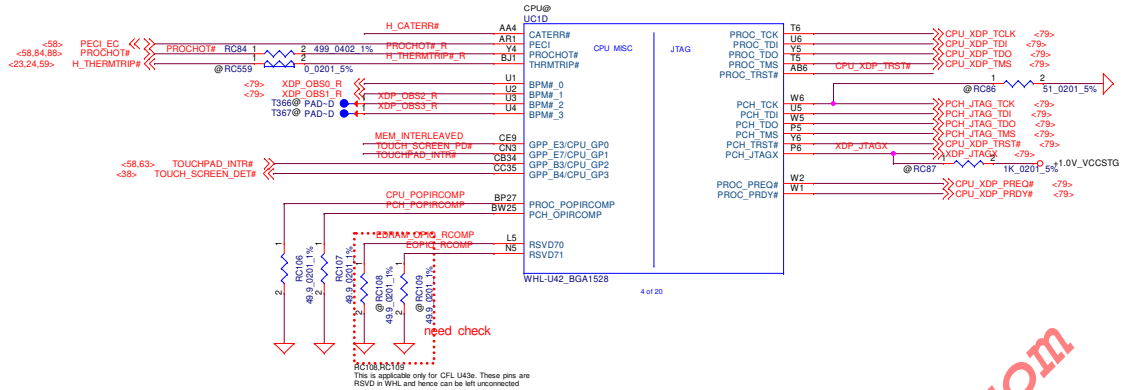
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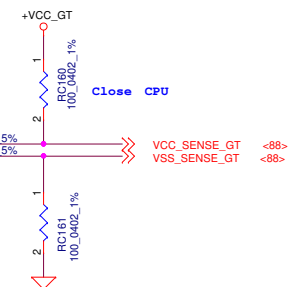
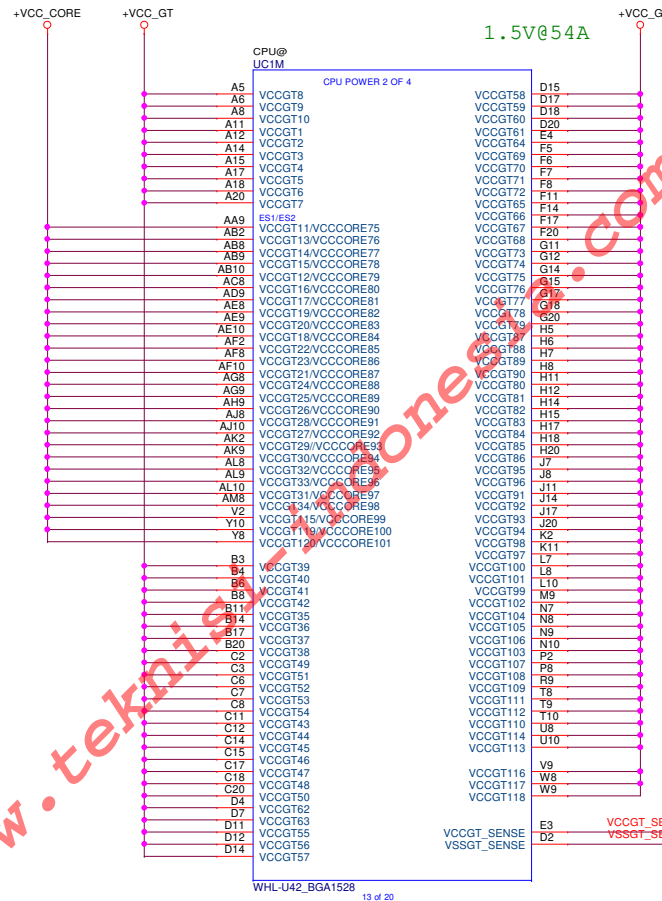
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## THE BALLOUT ONLY FOR WHL ES2 CPU

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCOORE
AB10	VCCGT	VCCGT	VCCOORE
AB2	VCCGT	VCCGT	VCCOORE
AB8	VCCGT	VCCGT	VCCOORE
AB9	VCCGT	VCCGT	VCCOORE
AC8	VCCGT	VCCGT	VCCOORE
AD9	VCCGT	VCCGT	VCCOORE
AE10	VCCGT	VCCGT	VCCOORE
AE8	VCCGT	VCCGT	VCCOORE
AE9	VCCGT	VCCGT	VCCOORE
AF10	VCCGT	VCCGT	VCCOORE
AF2	VCCGT	VCCGT	VCCOORE
AF8	VCCGT	VCCGT	VCCOORE
AG8	VCCGT	VCCGT	VCCOORE
AG9	VCCGT	VCCGT	VCCOORE
AH9	VCCGT	VCCGT	VCCOORE
AJ10	VCCGT	VCCGT	VCCOORE
AJ8	VCCGT	VCCGT	VCCOORE
AK2	VCCGT	VCCGT	VCCOORE
AK9	VCCGT	VCCGT	VCCOORE
AL10	VCCGT	VCCGT	VCCOORE
AL8	VCCGT	VCCGT	VCCOORE
AL9	VCCGT	VCCGT	VCCOORE
AM8	VCCGT	VCCGT	VCCOORE
V2	VCCGT	VCCGT	VCCOORE
Y10	VCCGT	VCCGT	VCCOORE
Y8	VCCGT	VCCGT	VCCOORE

**+VCCGT: 0.55~1.5V, 54A**  
**+VCCGTX : 0.55~1.5V, 7A**



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CPU(11/14)PWR-VCCGT

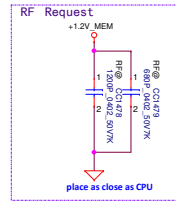
**LA-G871P**

1.0

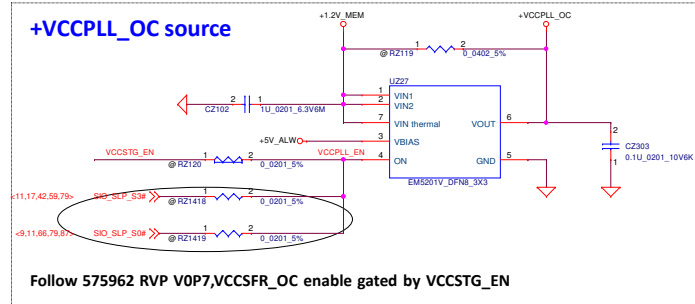
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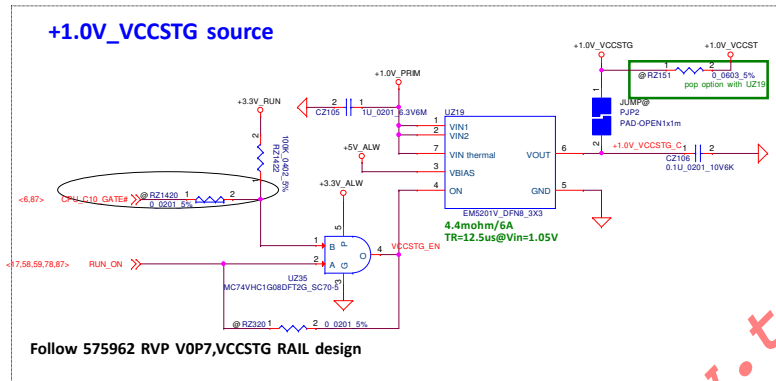
+1.2V\_DDR: 1.2V, 3.5A  
+1.0V\_VCCST: 1V, 120mA; VCCPLL: 1V, 120mA  
+1.0V\_VCCSTG: 1V, 40mA  
+VCCPLL\_OC: 1.2V, 260mA  
+1.0V\_VCCIO: 0.85~0.95V, 3.1A  
+VCC\_SA: 1.15V, 5.1A



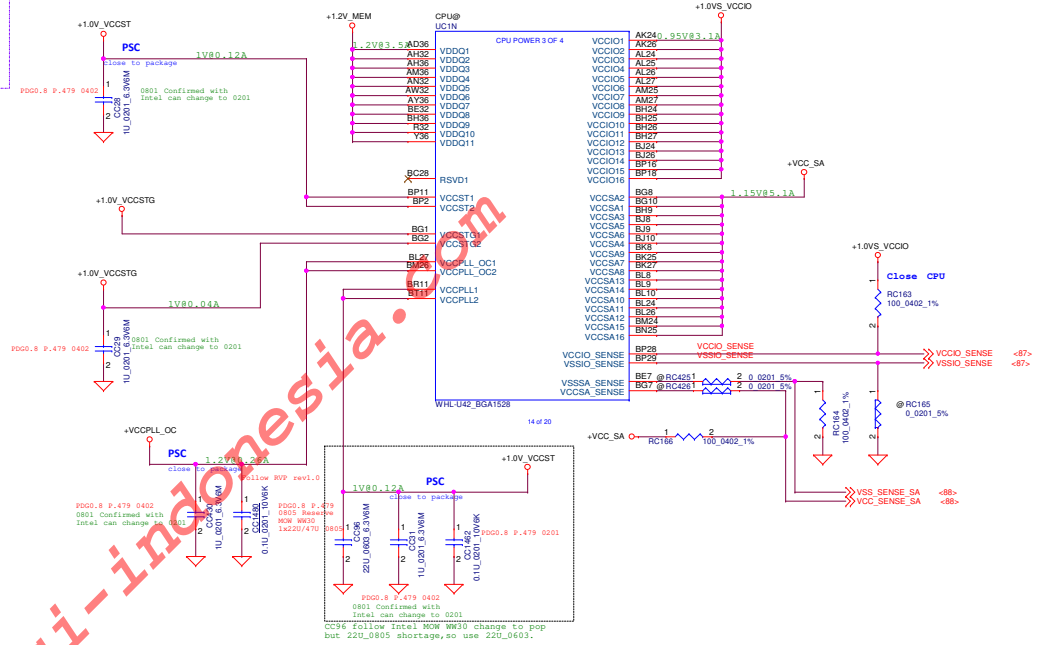
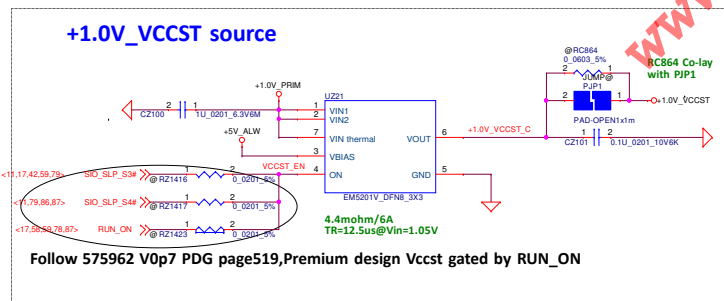
### +VCCPLL\_OC source



### +1.0V\_VCCSTG source

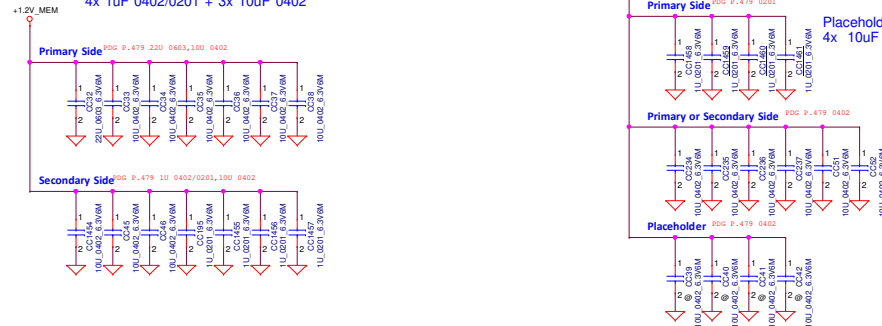


### +1.0V\_VCCST source



WHL U PDG rev0.8 P.479  
VDDQ:  
Primary Side cap  
1x 22uF 0603 + 6x 10uF 0402  
Secondary Side cap  
4x 1uF 0402/0201 + 3x 10uF 0402

WHL U PDG rev0.8 P.479  
VCCIO:  
Primary Side cap  
4x 1uF 0201  
Primary or Secondary Side  
6x 10uF 0402  
Placeholder Only  
4x 10uF 0402



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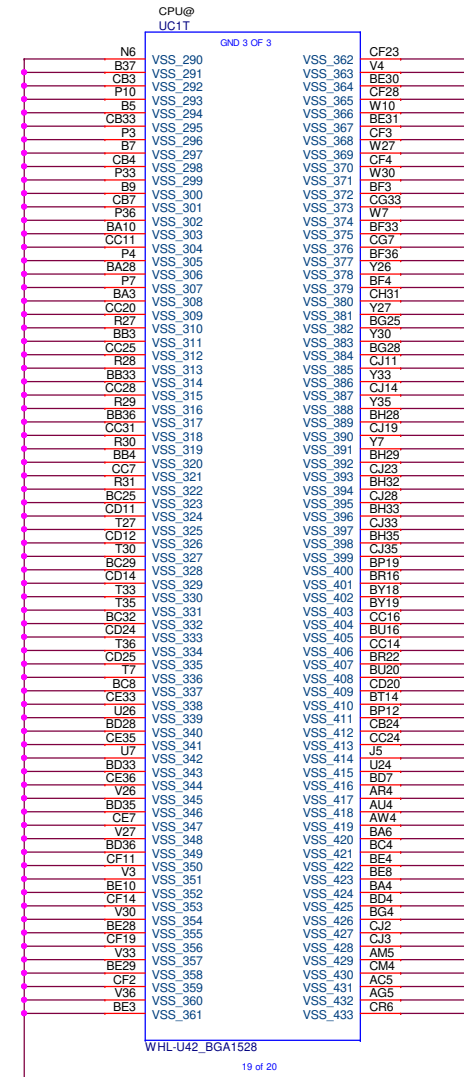
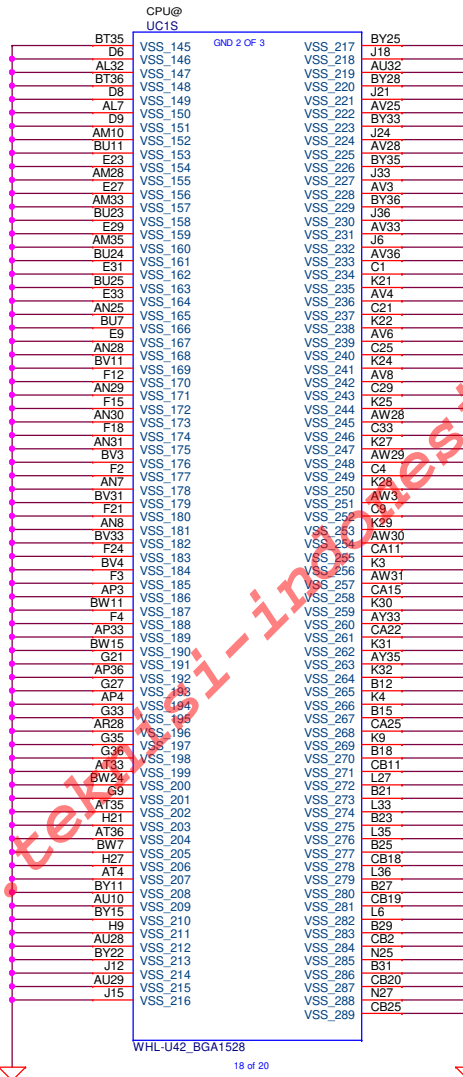
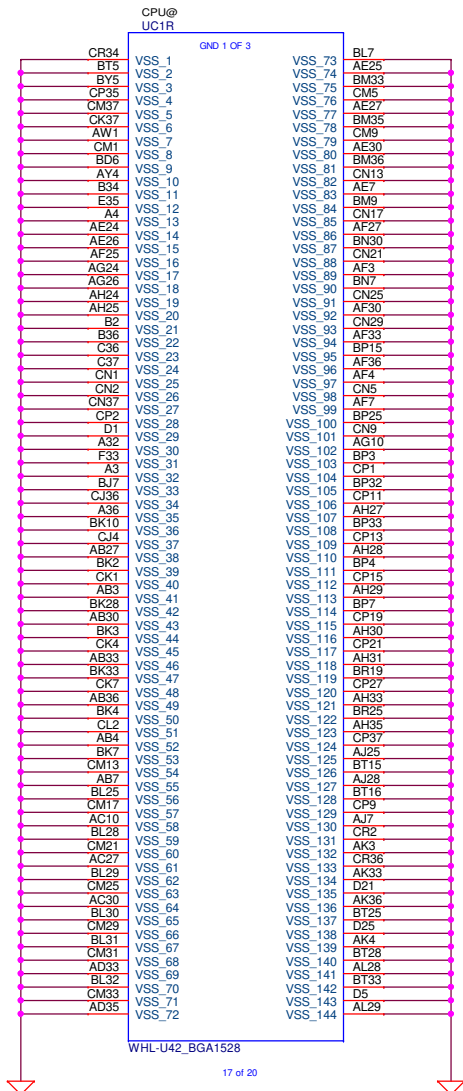
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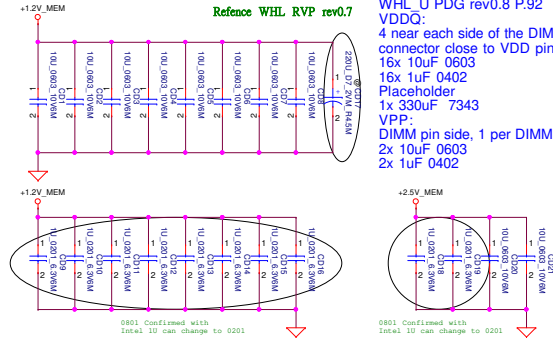


<7> DDR\_A\_DQS[0..7] <<>>  
 <7> DDR\_A\_DQ[0..63] <<>>  
 <7> DDR\_A\_DQS[0..7] <<>>  
 <7> DDR\_A\_MA[0..16] <<>>

Layout Note:  
Place near JDIMM1

Merion Limit height  
CD17 change to SGA0000AM00 H=1.0mm(MAX)

Reference WHL RVP rev0.7

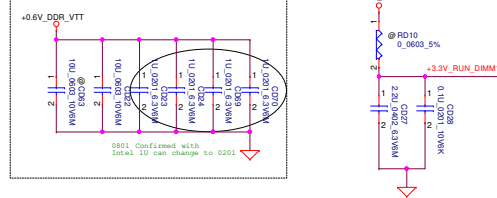


WHL\_U PDG rev0.8 P.92

VTT:  
Place on VTT plane close to SODIMM  
2x 10uF 0603(1 cap stuffed, 1 placeholder)  
4x 1uF 0402  
VDDSPD:  
Place close to DIMM  
2x 0.1uF 0402  
2x 2.2uF 0402

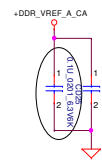
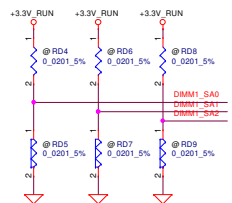
Layout Note:  
Place near JDIMM1.258

Reference WHL RVP rev0.7



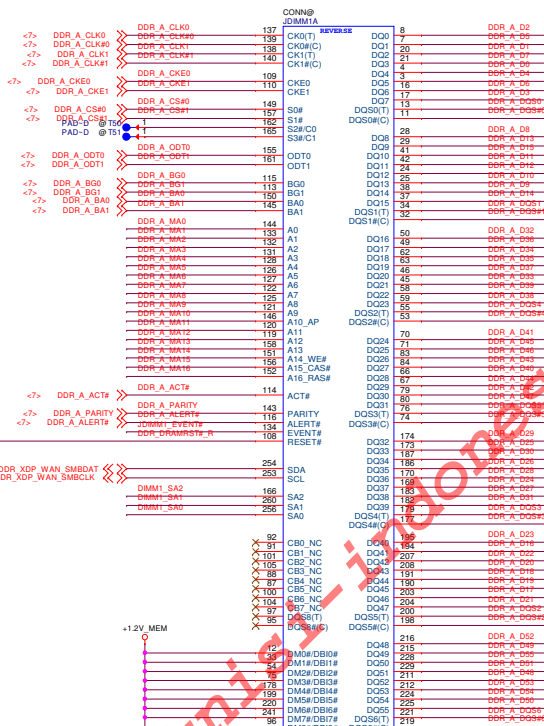
## DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

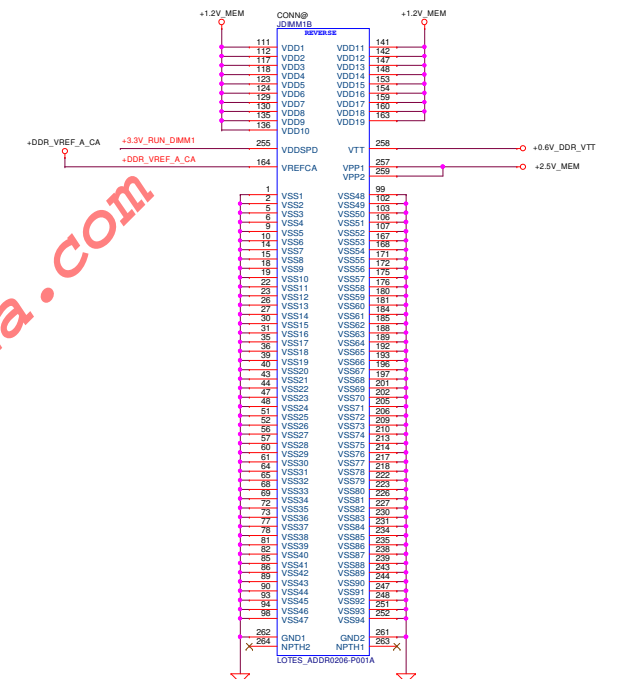


<24> DDR\_DRAMRST#\_R @RD12 1 2 0.0201 5% DDR\_DRAMRST# <<DDR\_DRAMRST# <7>

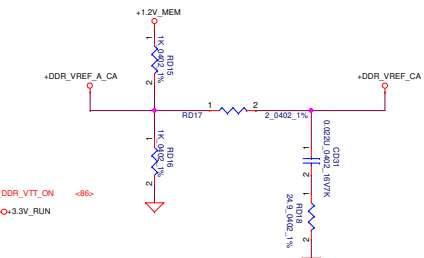
Link LOTES\_ADDR0206-P001A02 done 0410



LOTES\_ADDR0206-P001A



JDIMM1\_EVENTS# 1 2 1K\_0402\_5% <<H\_THERMTRIP# <14.24.55>



6/8 Change to SA00007WE00 DII

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DGPU			
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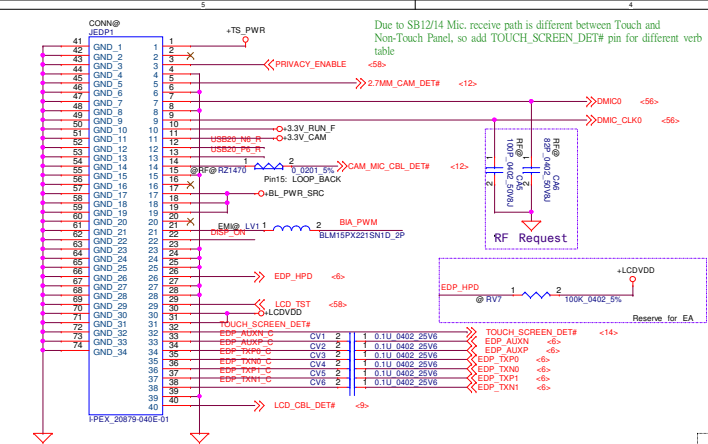
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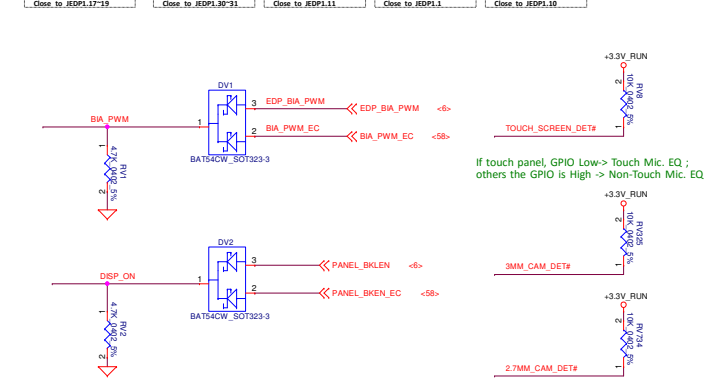
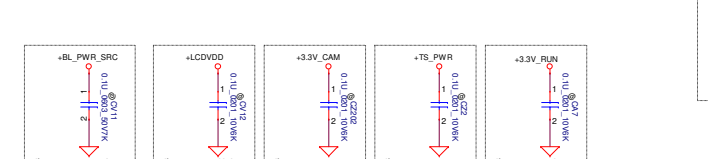
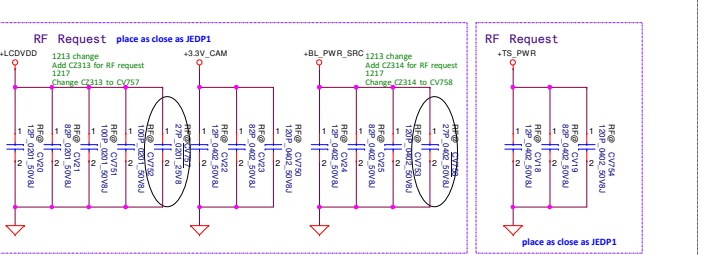
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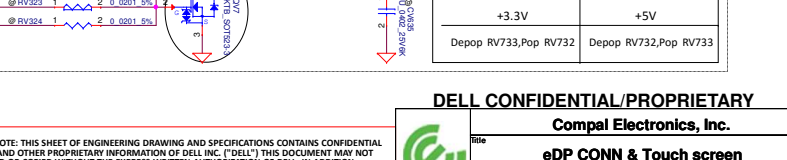
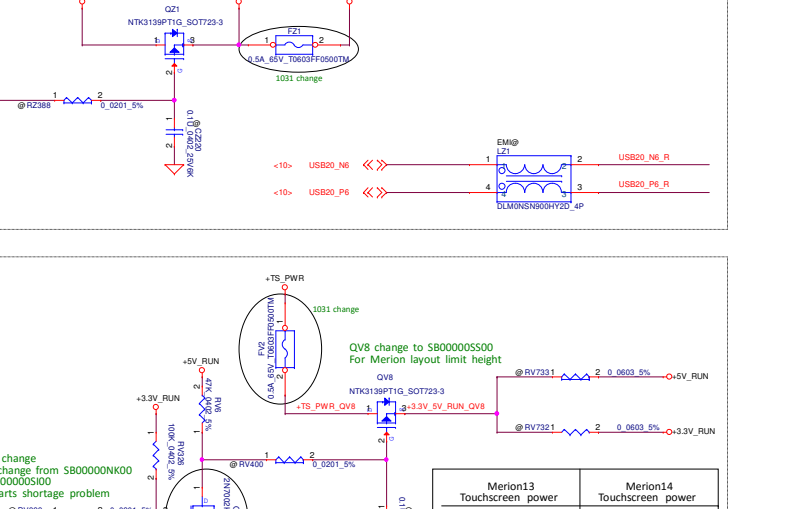
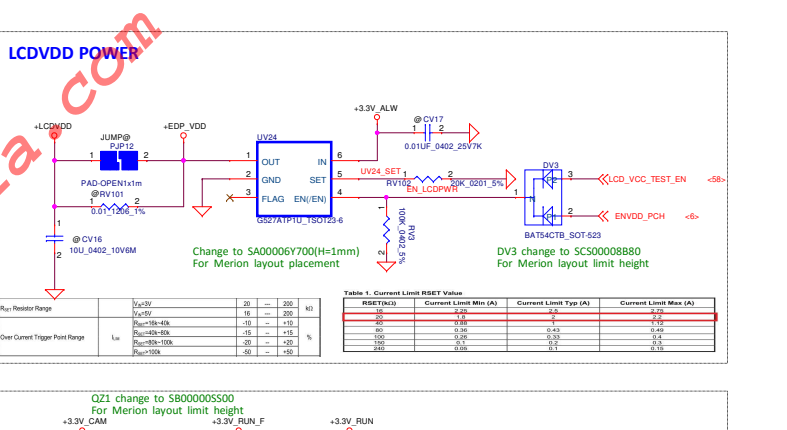
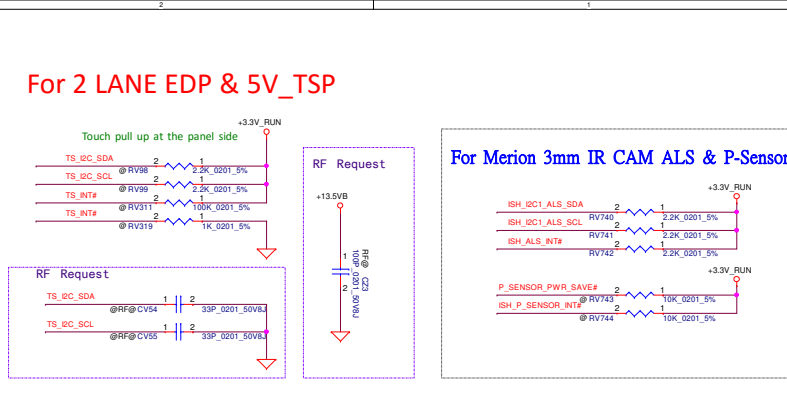
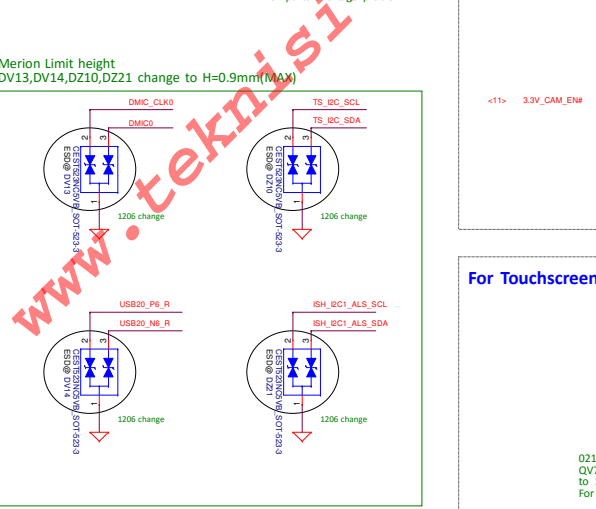
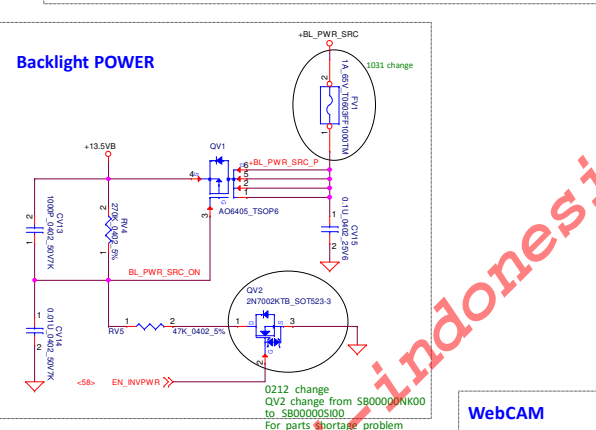
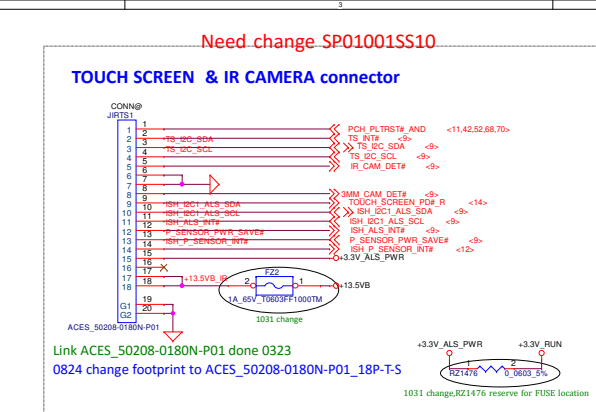
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Relink I-PEX\_20879-040E-01 done 0827



Camera Truth table	Mic Only	6mm Normal Camera	6mm IR Camera	3mm IR Camera	2.7mm HD Camera
GPP_G0(CAM_MIC_CBL_DET#)	H	L	L	L	L
GPP_D9(IR_CAM_DET#)	H	H	L	H	H
GPP_C20(3MM_CAM_DET#)	H	H	H	L	H
GPP_A16(2.7MM_CAM_DET#)	H	H	H	H	L
Antenna Location	Bottom	Top	Top	Bottom	Bottom



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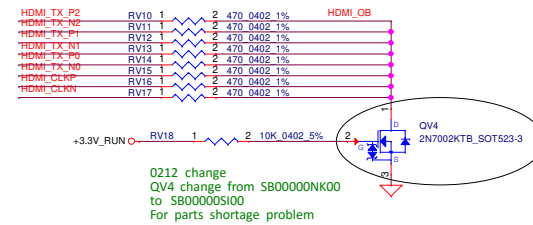
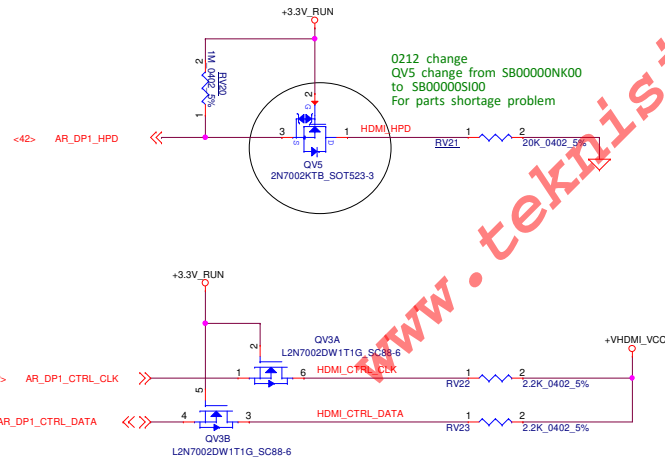
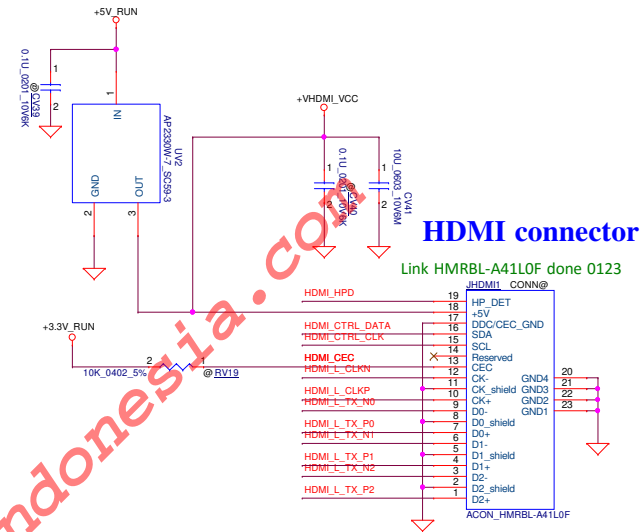
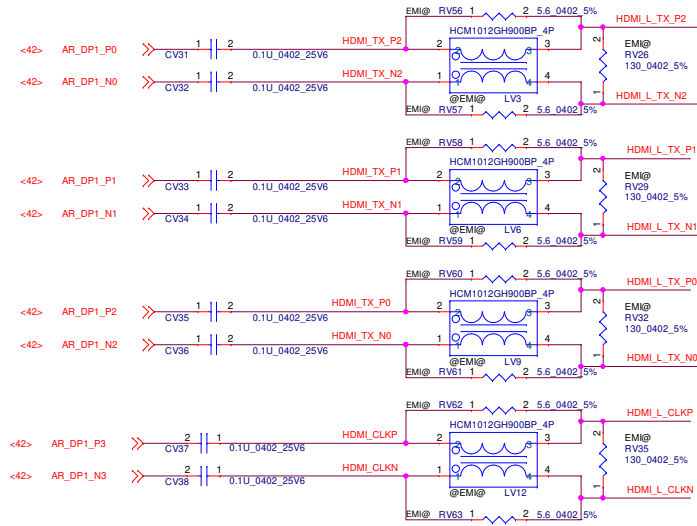
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Based on EMI & EE test result  
Change location LV31-LV38 to 5.60hm  
RV26,RV29,RV32,RV35 to 130Ohm



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	<b>Compal Electronics, Inc.</b>			
	Title			
	<b>HDMI CONN</b>			
	Size	Document Number	Rev	
		<b>LA-G871P</b>	<b>1.0</b>	
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# Reserve

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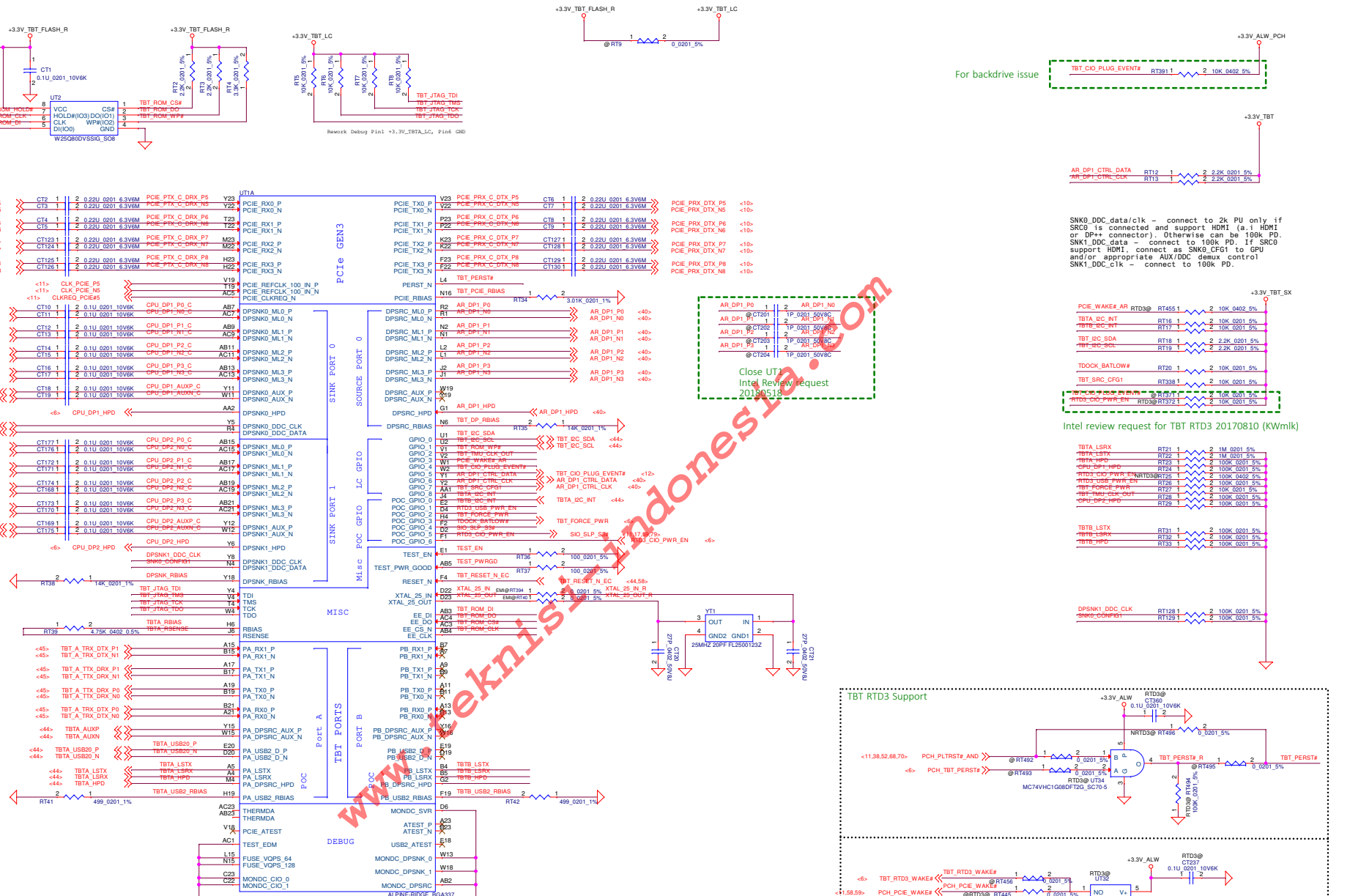
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Size	Document Number		Rev
	LA-G871P		1.0
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CPU DD11

CPU DD12

Type C

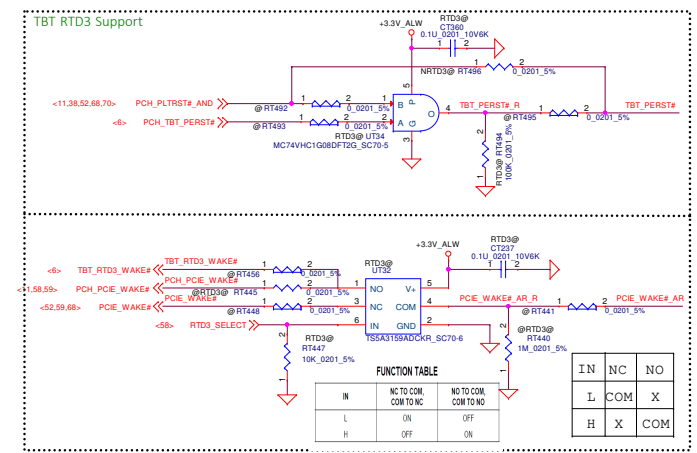


For backdrive issue

SNK0 DDC\_data/cclk - connect to 2k PU only if SRC0 is connected and support HDMI (a.i HDMI or DP++ connector). Otherwise can be 100k PU. SNK1 DDC\_data - connect to 100k PU. If YC0 support HDMI, connect as SNK0 CF01 to GPU and/or appropriate AUX/DOC demux control SNK1 DDC\_clk - connect to 100k PU.

Close UT13  
Intel Review request  
20180518

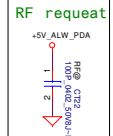
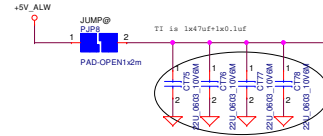
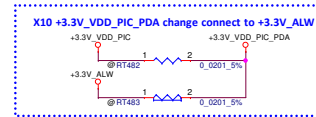
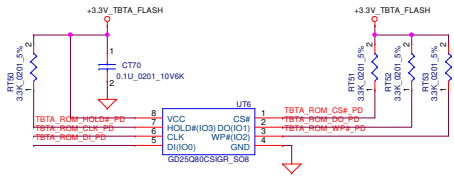
Intel review request for TBT RTD3 20170810 (kWmlik)



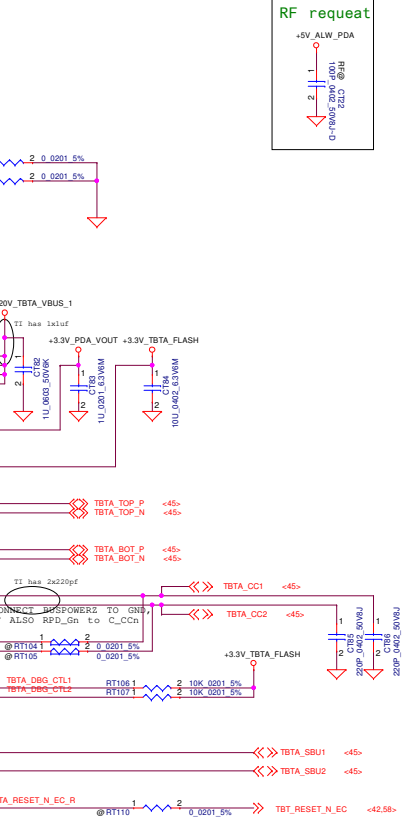
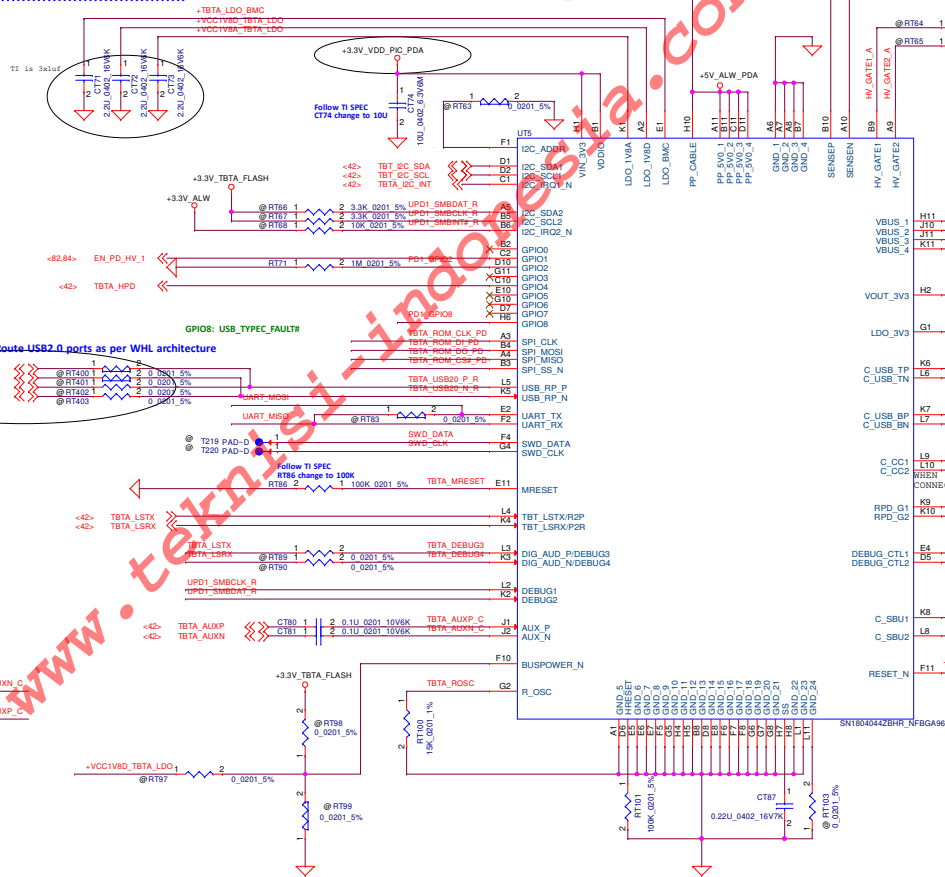
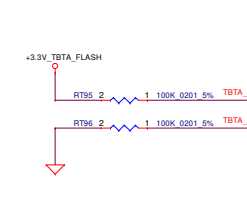
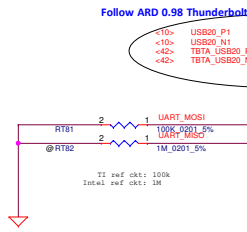
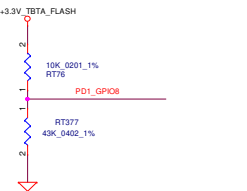
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For AR port1



DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.20	0.28	2	UFP only 5V @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

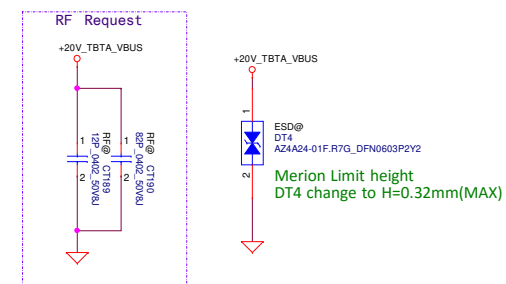
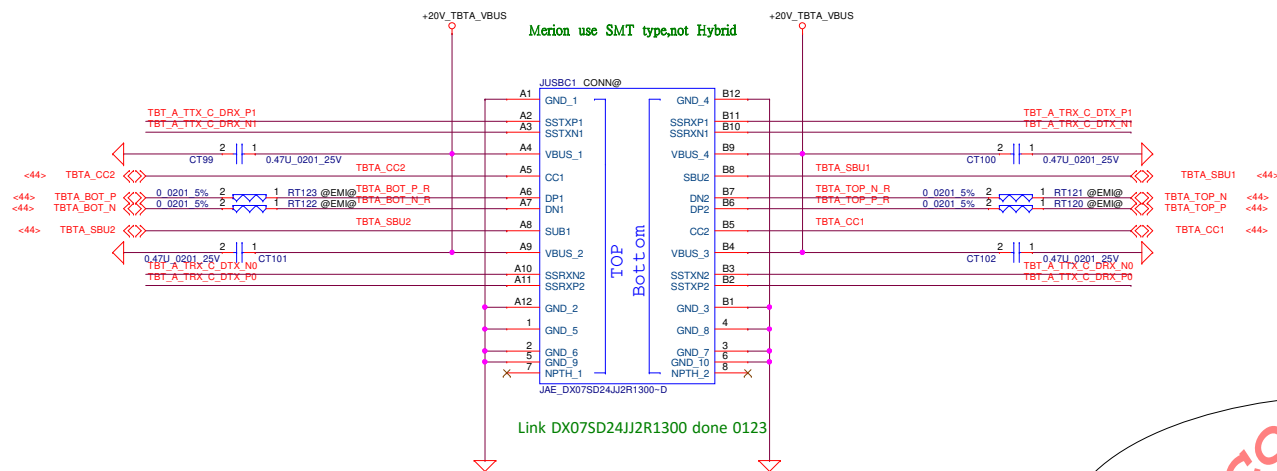


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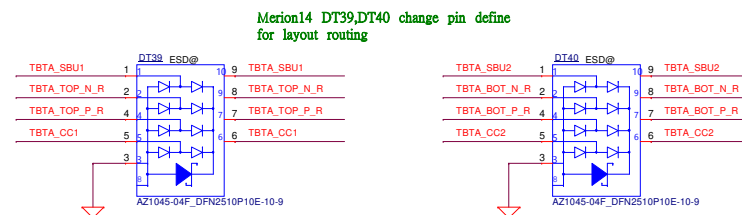
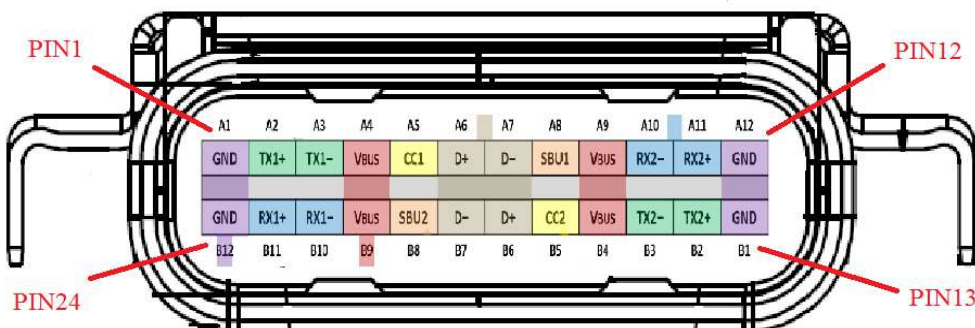
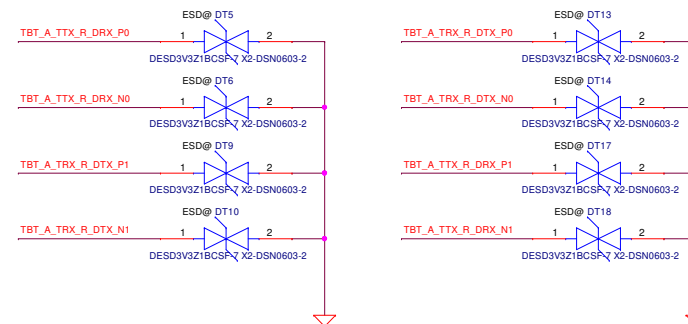
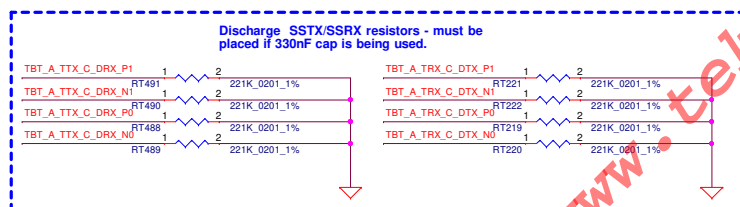
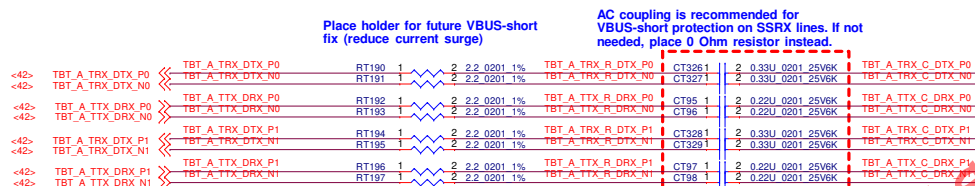
Compal Electronics, Inc.	
Type CIPD Controller TI	
LA-G871P	Rev 1.0
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Remove Low Speed VBUS-Short Protection




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Title		TYPE-C Port2 (1/2)	
Size	Document Number	LA-G871P	Rev 1.0
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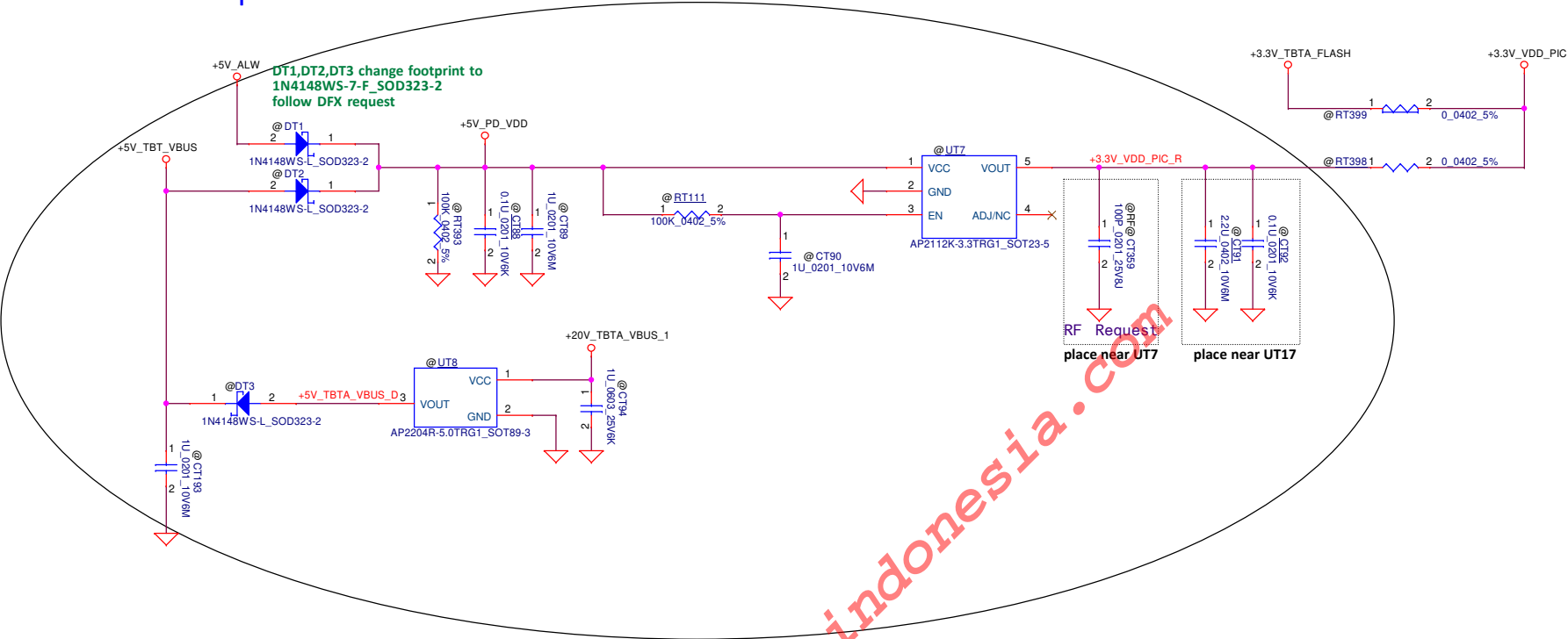
Compal Electronics, Inc.



Title		
TYPE-C Port3 (2/2)		
Size	Document Number	Rev
	LA-G871P	1.0
Date:	Tuesday, March 05, 2019	Sheet 49 of 109

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Reserve for external PD power



1031 change

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Compal Electronics, Inc.




Title		[Type C]PD Power	
Size	Document Number	LA-G871P	
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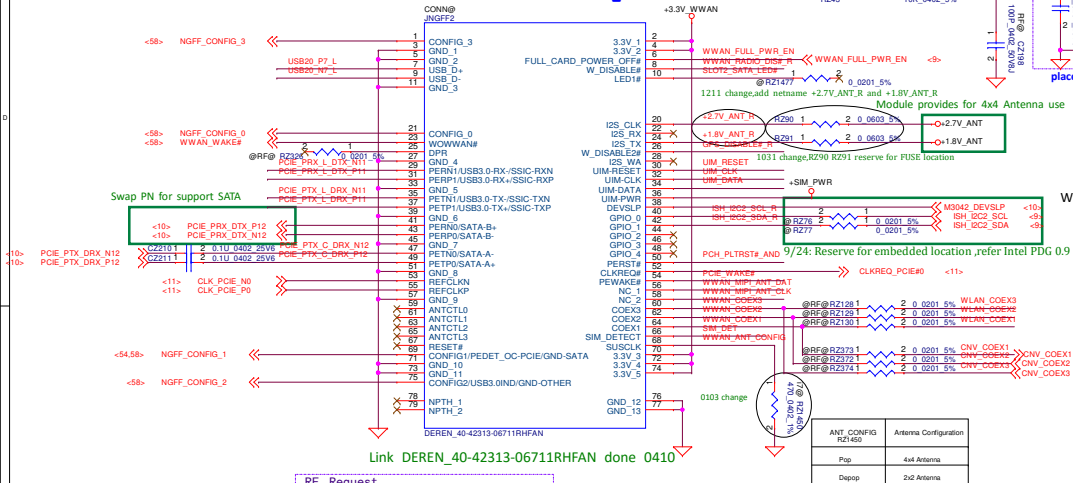
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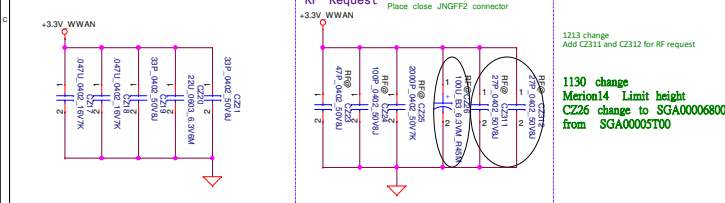
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Size	Document Number		Rev
	LA-G871P		1.0
Date:	Tuesday, March 05, 2019		Sheet 51 of 109

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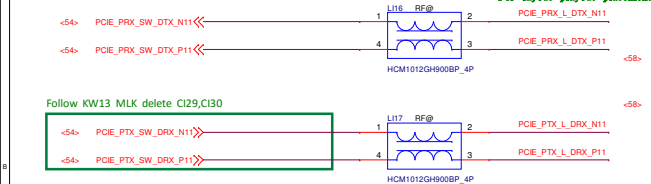
NGFF slot B Key B



Link DEREN\_40-42313-06711RHFAN done 0410



Merion14 swap LI16,LI17 net for layout routing

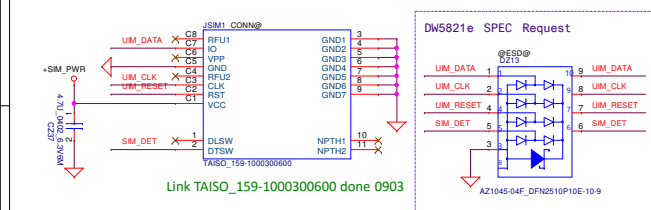


Merion delete RI27~RI30  
For layout playout placement

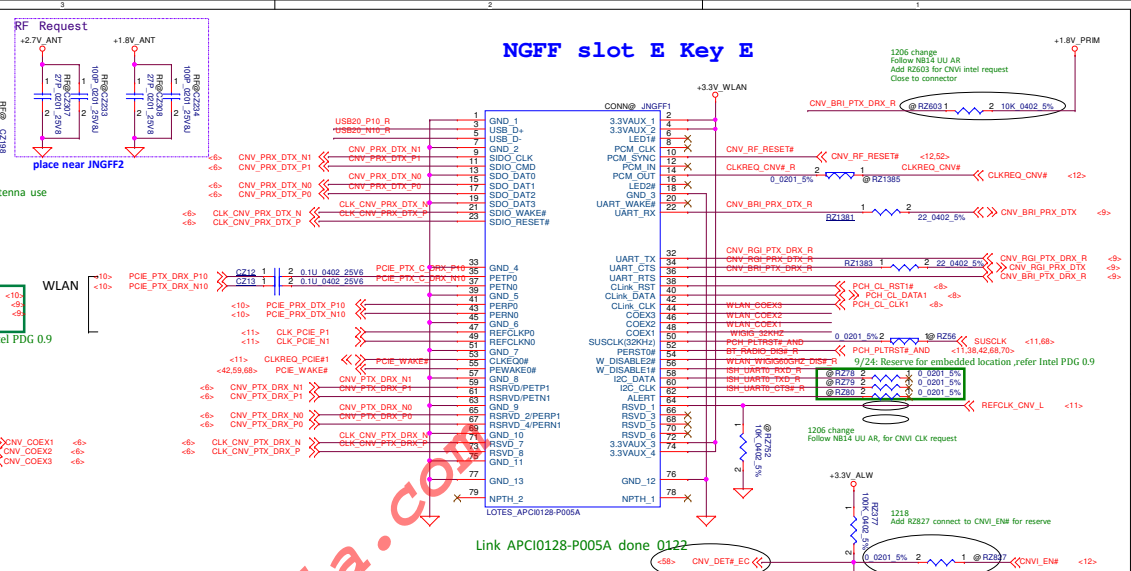
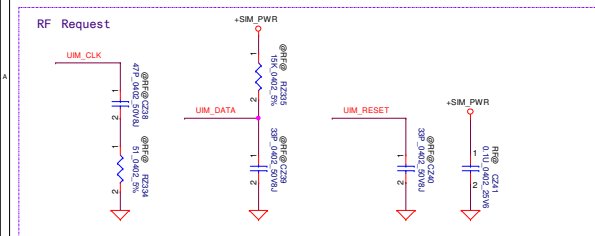
Follow KW13 MLK delete CI29,CI30



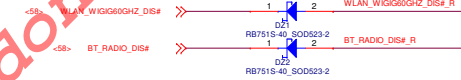
## SIM Card Push-Push



Link TAISO\_159-1000300600 done 0903



Link APCI0128-P005A done 0122



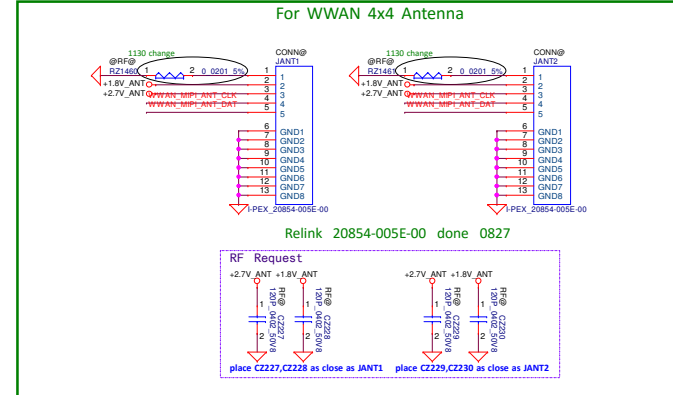
WWAN MIPI ANT DAT and WWAN MIPI ANT CLK

(1) The trace length  $< 30\text{cm}$

This max length guidance is practical level of definition

(2) Spacing to all other signal need  $4 \times$  line width

For WWAN 4x4 Antenna



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M3042_PCIE#_SATA
	GND	GND	GND	GND	SSD.SATA	High
	GND	HIGH	GND	GND	SSD_PCIE(2 lane)	Low
	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA_PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

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Title	NGFF Card
NGFF Card	

Size	Document Number
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LA-G871P

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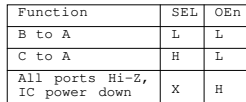
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[illegible]

STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M3042_PCIE#_SATA#
0	GND	GND	GND	GND	SSD-SATA	HIGH
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	LOW
8	HIGH	GND	GND	GND	WWAN	LOW
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	LOW
15	HIGH	HIGH	HIGH	HIGH	NA	LOW

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	<b>Compal Electronics, Inc.</b>		
	Title		
	<b>USB/PCIE MUX HD3SS3212</b>		
	Size	Document Number	Rev 1.0
<b>LA-G871P</b>			
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# Reserve

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Compal Electronics, Inc.

Title

Reserve for PCIE device

Size

Document Number

LA-G871P

Rev

1.0

Date:

Tuesday, March 05, 2019

Sheet

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of

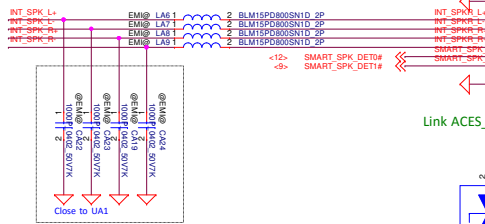
109

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1W x 1ch, 4ohm (Transducer spec is 80hm/0.5Watt per unit, there are two transducer units in one speaker box)

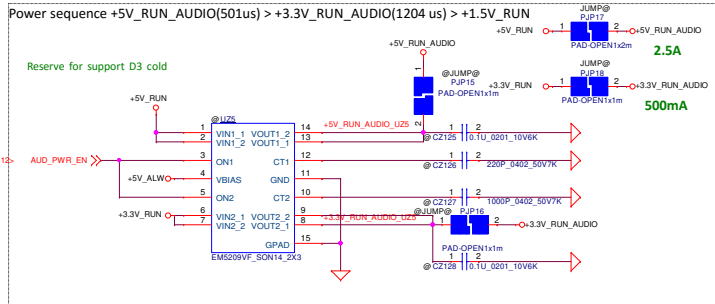
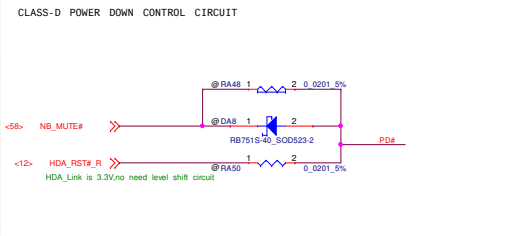
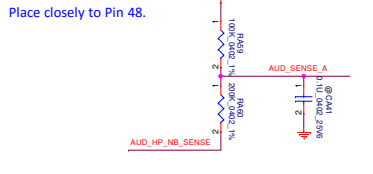
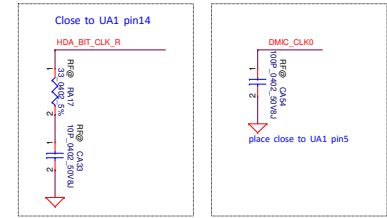
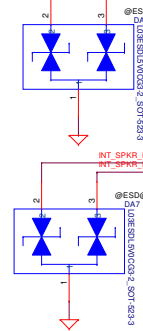
## Internal Speakers Header

40 mils trace keep 20 mil spacing



Only Merion14 support 3 vendor

Link ACES\_50278-00801-001 DONE 0809



Smart Amp Vendor	Vendor1 rg	Vendor2 Zytex	Vendor3 Zytex
SMART_SPK_DET0# (PCH_GPP_C71)	High	Low	High
SMART_SPK_DET1# (PCH_GPP_C22)	High	High	Low

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<12> HDA\_BIT\_CLK\_R  
<12> HDA\_SDOUT\_R  
<12> HDA\_SDO0

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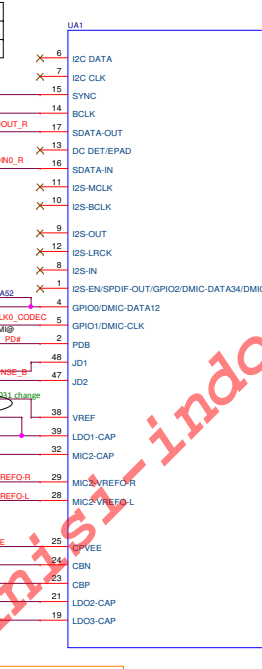
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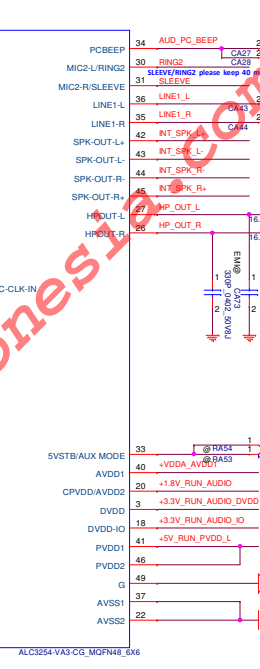
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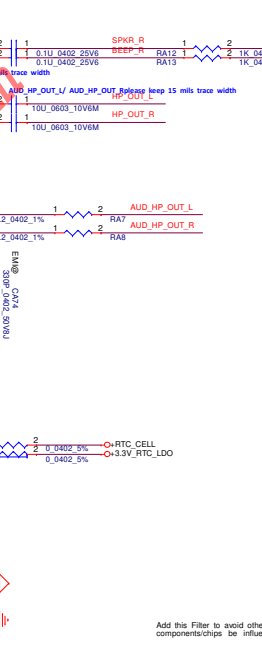
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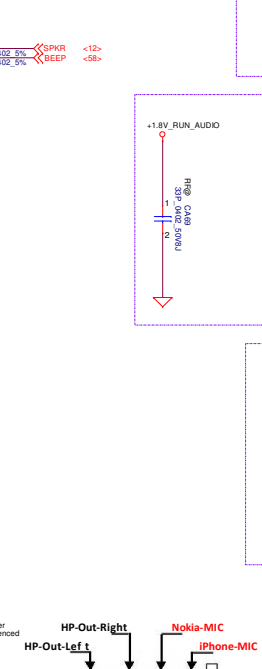
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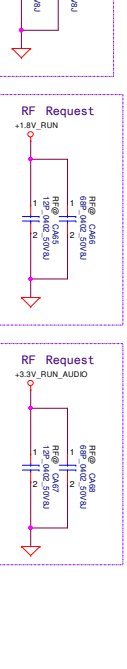
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# Reserve

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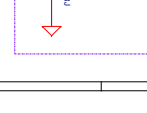
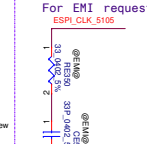
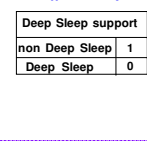
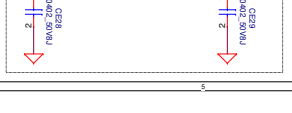
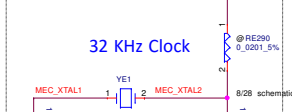
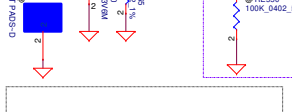
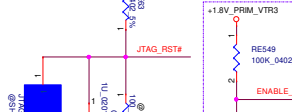
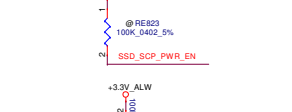
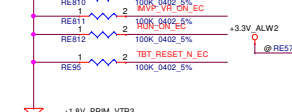
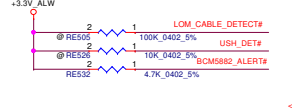
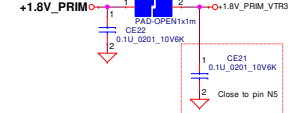
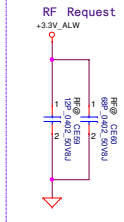
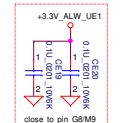
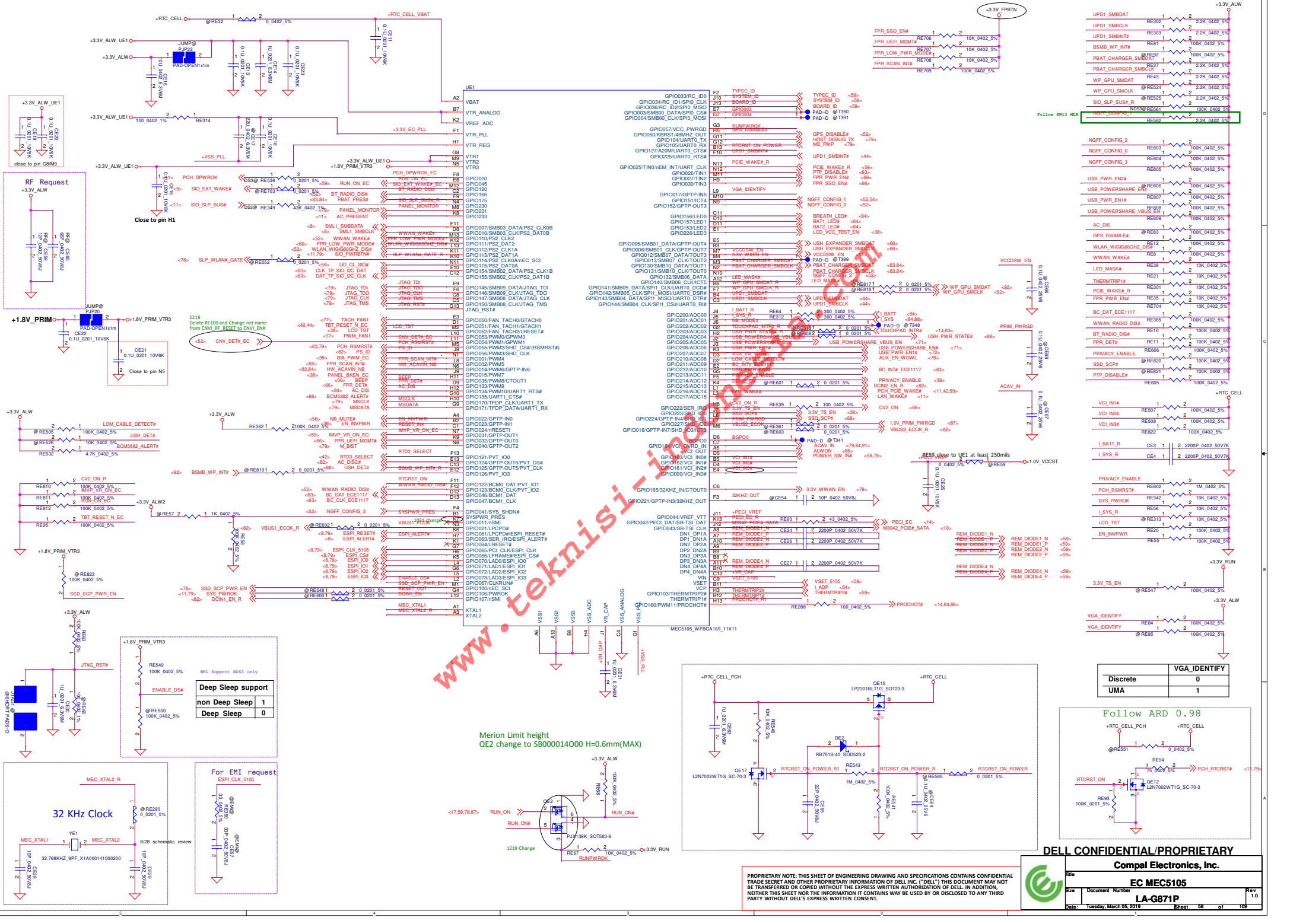
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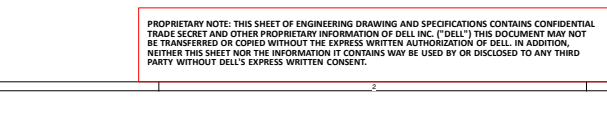
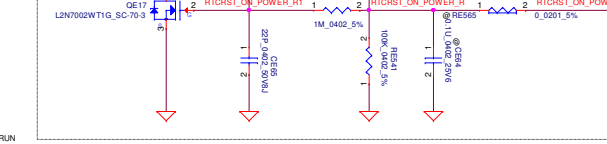
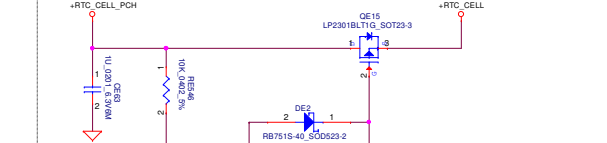
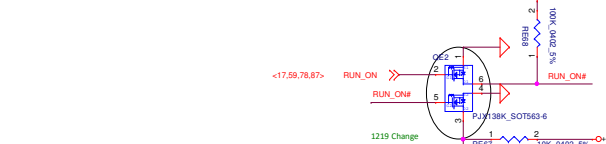


Title		Audio Ampfilter	
Size	Document Number		Rev
Date: Tuesday, March 05, 2019		Sheet 57 of 109	1.0

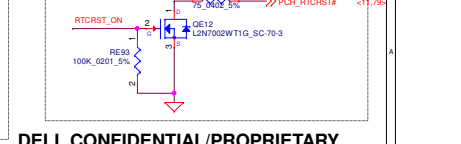
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Merion Limit height  
QE2 change to S8000014000 H=0.6mm(MAX)



VGA_IDENTIFY	
Discrete	0
UMA	1



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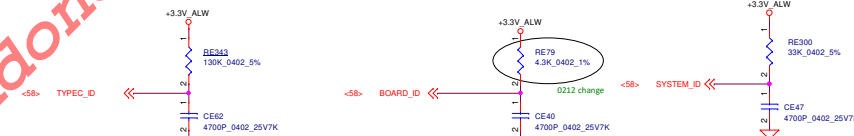
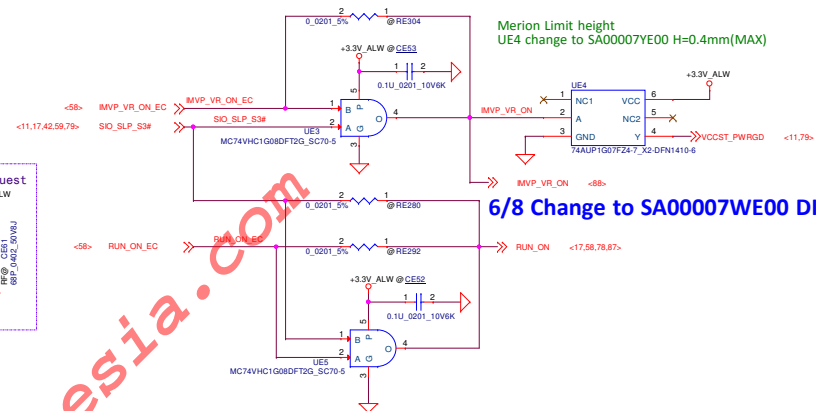
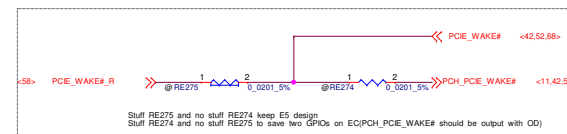
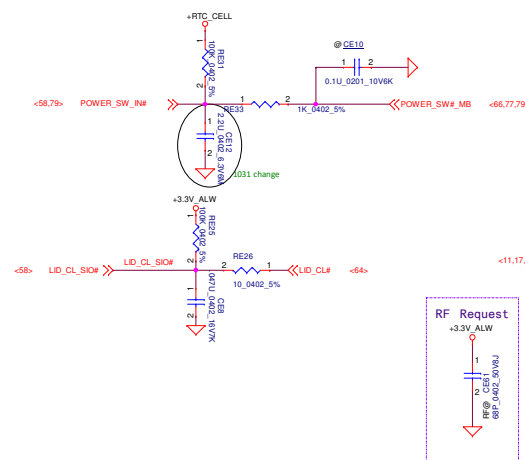
Compal Electronics, Inc.

EC MEC5105

LA-G871P

Rev 1.0

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RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
* 130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	
2K	4700p	
1K	4700p	

RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	reserved
* 4.3K	4700p	A00
2K	4700p	
1K	4700p	

RE300	CE47	PANEL SIZE
240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
* 33K	4700p	14"
8.2K	4700p	15"
4.3K	4700p	17"
2K	4700p	15P
1K	4700p	

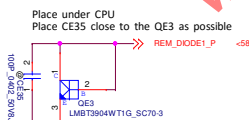
TYPEC\_ID rise time is measured from 0%~63.2%.

BOARD\_ID rise time is measured from 0%~63.2%.

SYSTEM\_ID rise time is measured from 0%~63.2%.

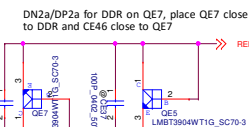


5085 Channel	Locat i on
DP1/DN1	CPU (QE3)
DP2/DN2	2280 SSD (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

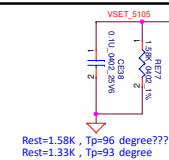
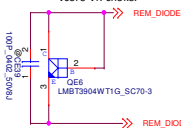


DP2/DN2 for WiGig on QE5, place QE5 close to WiGig and CE37 close to QE5

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.



DN2a/DP2a for DDR on QE7, place QE7 close to DDR and CE46 close to QE7



Rest=1.58K, Tp=96 degree???

Rest=1.33K, Tp=93 degree

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Rev	MEC5105 support	Rev	1.0
Date	Tuesday, March 05, 2019	Sheet	58 of 109

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# Reserve

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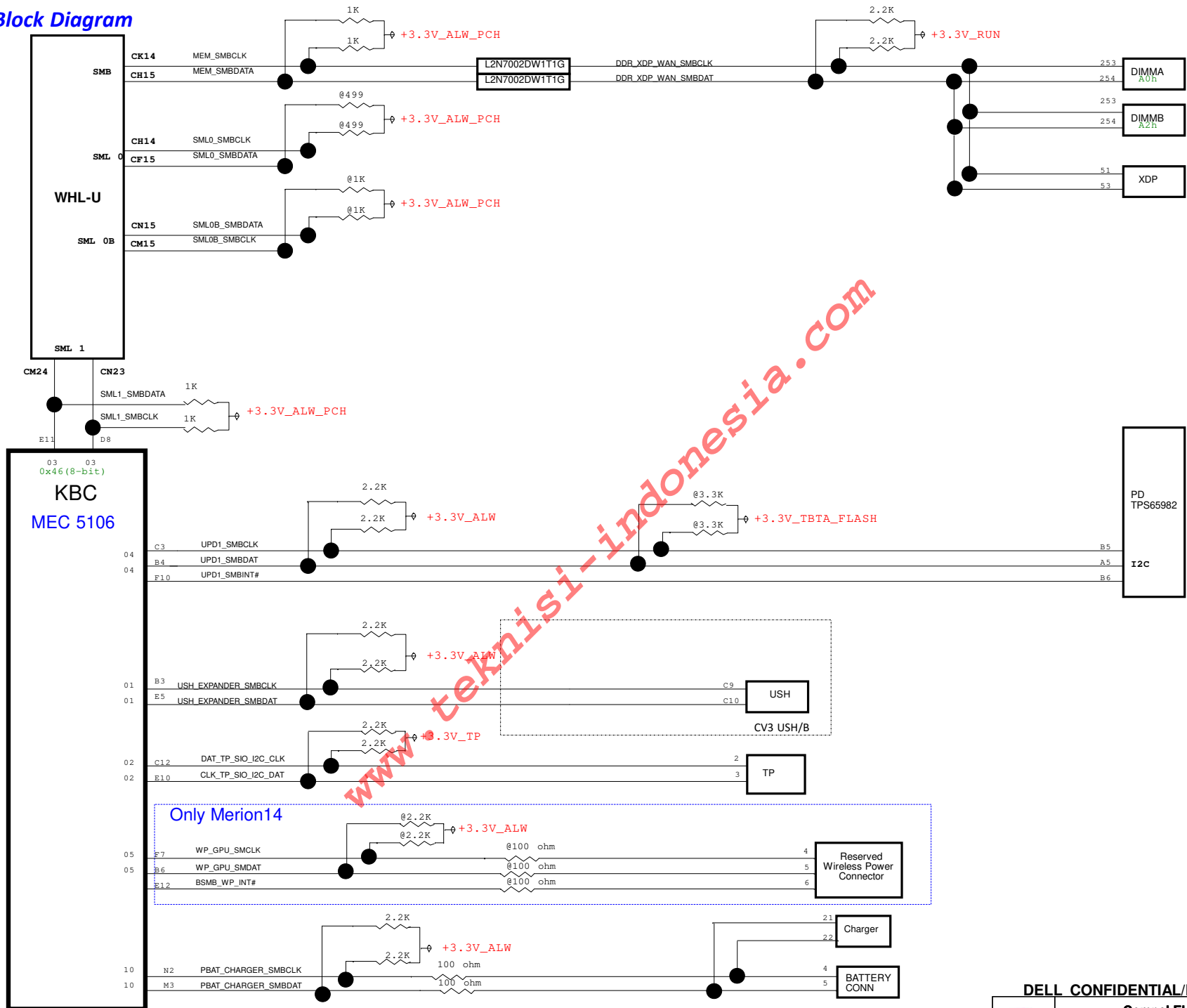
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		Compal Electronics, Inc.	
Title		Secure & Reset IC	
Size	Document Number		Rev
	LA-G871P		1.0
Date:	Tuesday, March 05, 2019		Sheet 60 of 109

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# Merion SMBus Block Diagram



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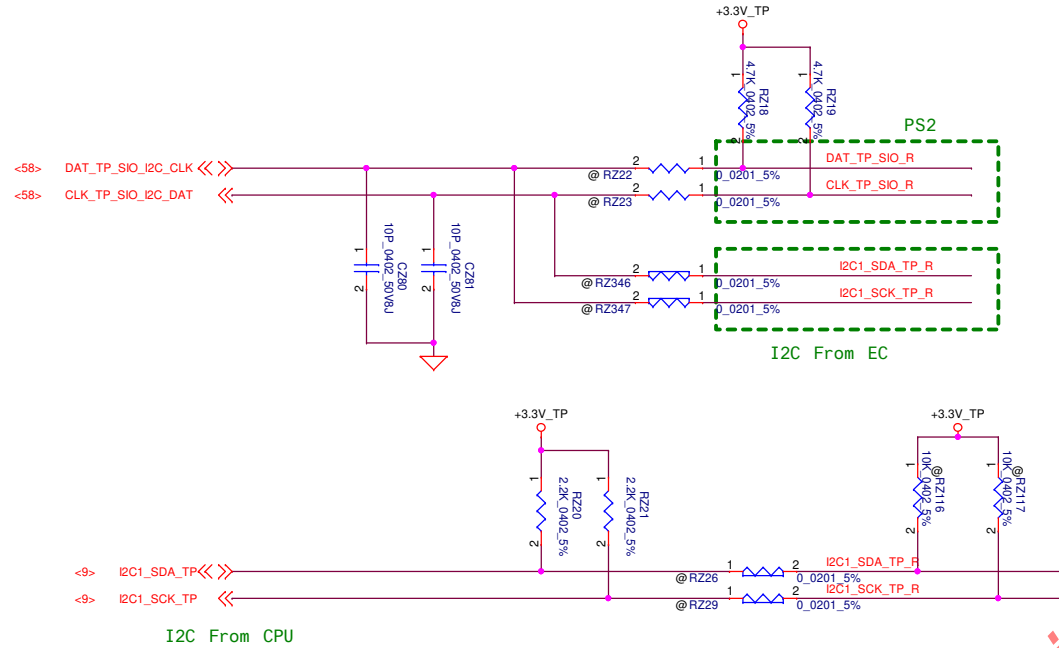
Compal Electronics, Inc.



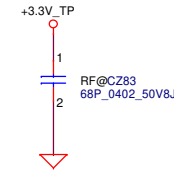
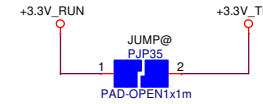
Title		LEDs (Controller)	
Size	Document Number		Rev
	LA-G871P		1.0
Date:	Tuesday, March 05, 2019	Sheet	62 of 109

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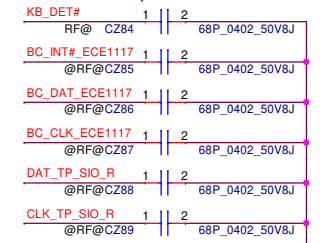
## Touch Pad



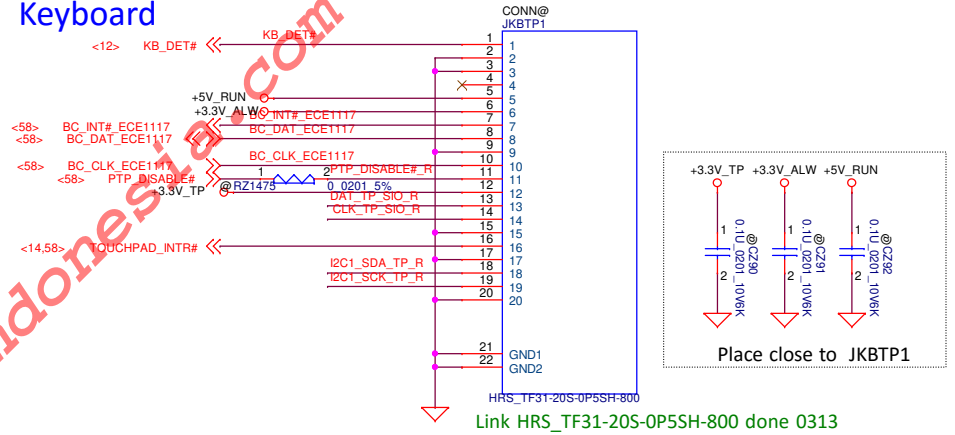
Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)  
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows  
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues



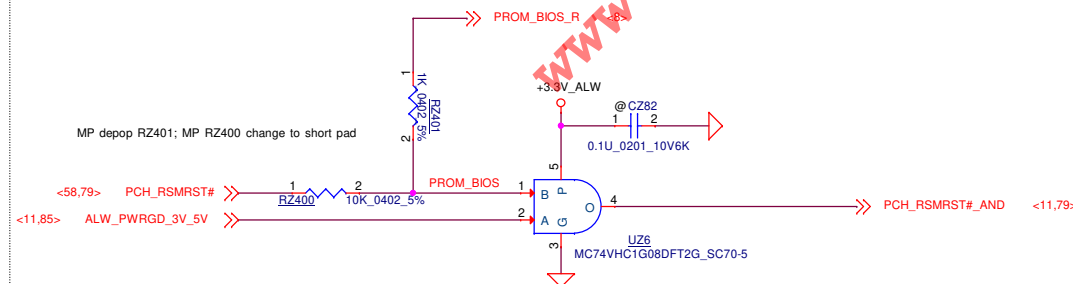
## RF Request



## Keyboard



## RSMRST circuit



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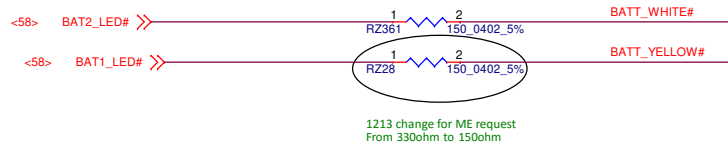
Keyboard

LA-G871P

Date: Tuesday, March 05, 2019 Sheet 63 of 109

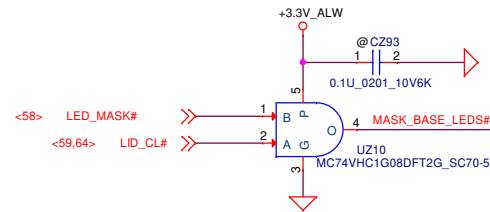
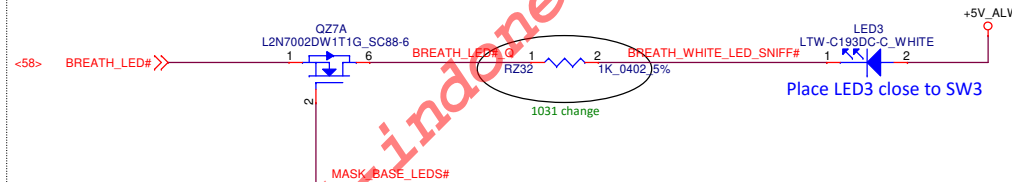
Rev 1.0

## Battery LED

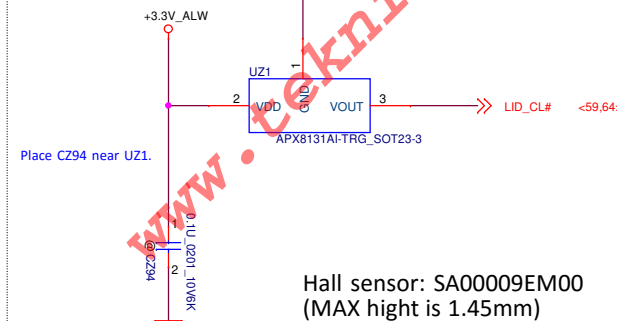


## Breath LED for Merion 14

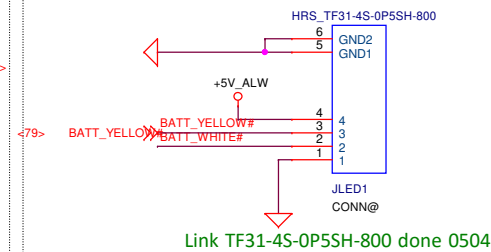
LED P/N change to SC50000FL00 from SC50000BA00



## LID SWITCH



## LED board CONN



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Title		LED & LID	
Size	Document Number	LA-G871P	
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Rev		1.0	

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# Reserve

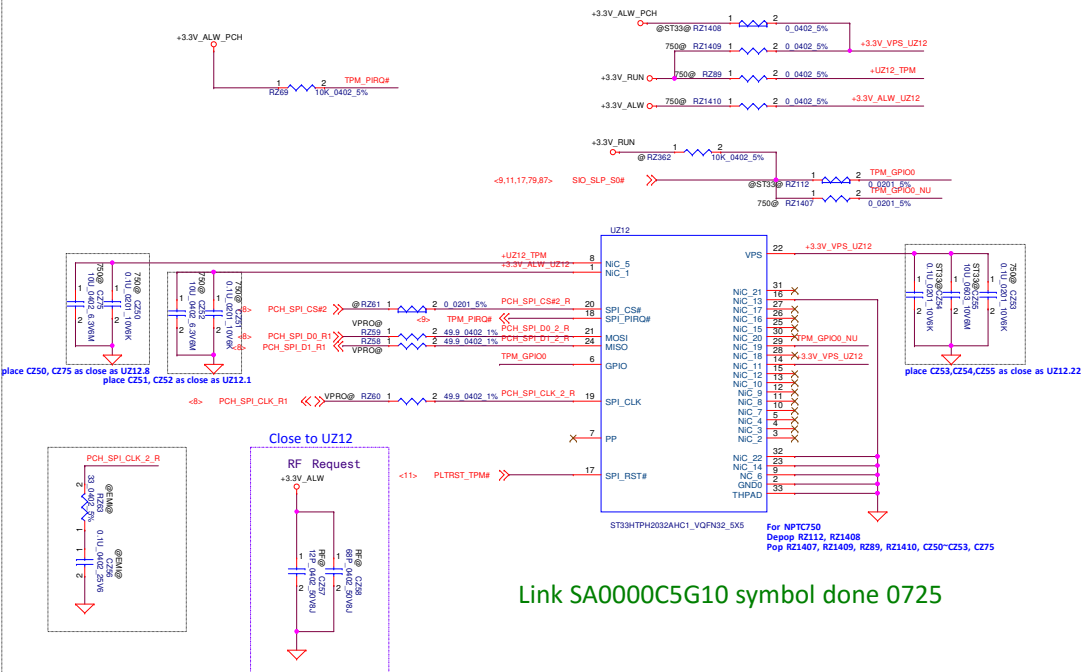
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Title		
Reserve for KB/TP/LED/LID		
Size	Document Number	Rev
	LA-G871P	1.0
Date:	Tuesday, March 05, 2019	Sheet 65 of 109

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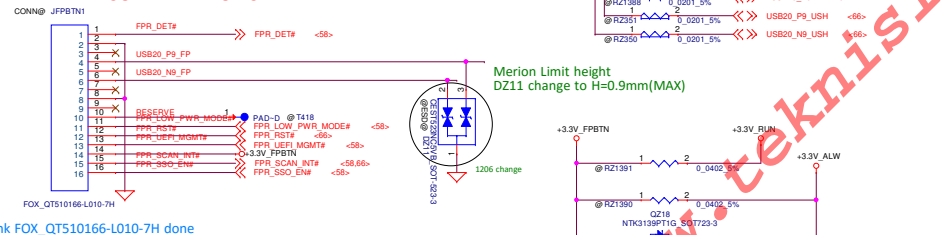
For ST/Nuvoton TPM



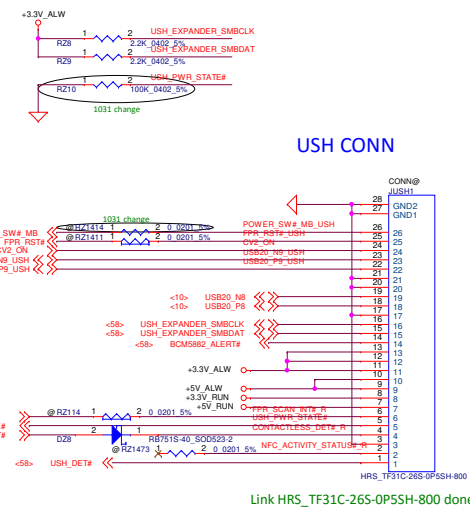
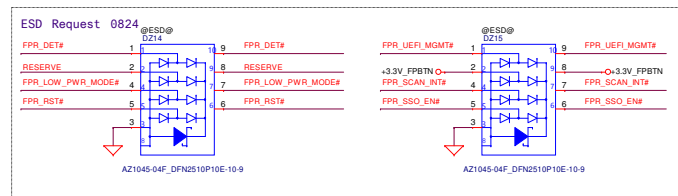
Link SA0000C5G10 symbol done 0725

**FP in PWR BUTTON connector**

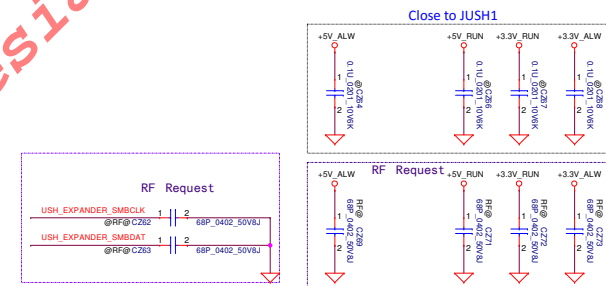
NEED CONFIRM MODULE PINDEFINE



Compal MB CONN Symbol	Signal	FPR Symbol
2	GND	2
4	USB DP(D+)	1
6	USB DM(D-)	3
8	GND	4
10	RESERVED	5
12	FP RESET#	6
14	+3.3V_FPBTN	7
16	FPR_SSO_EN#	8
15	FPR_SCAN_INT#	9
13	FPR_UFEL_MGMT#	10
11	FPR_LOW_PWR_MODE#	11
9	NA	12
7	NA	13
5	NA	14
3	NA	15
1	FPR DET(GND)	16



Link HRS\_TF31C-26S-0P5SH-800 done 0313



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## SH & TPM


**LA-G871P**

Date: Tuesday, March 05, 2019 Sheet 66 of 109

# Reserve

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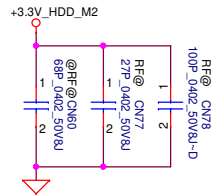
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Title		
HDD/ODD/FFS Connector		
Size	Document Number	Rev
	LA-G871P	1.0
Date:	Tuesday, March 05, 2019	Sheet 67 of 109

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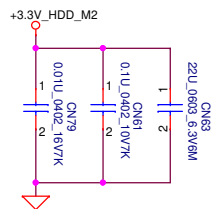
# Add Power Decoupling for support Intel Teton Glacier

## RF Request

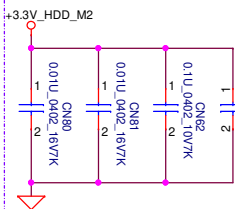


Place near JNGFF3

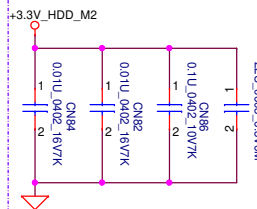
## Place close JNGFF3 pin 12,14,16,18



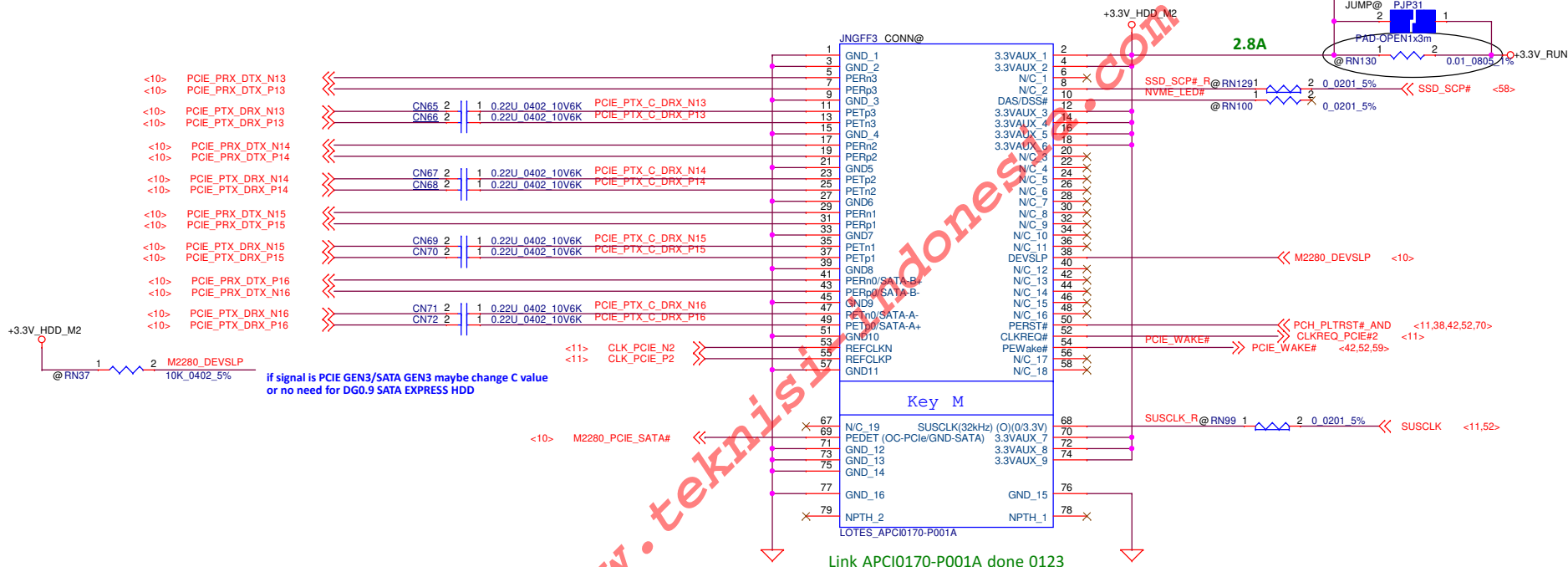
## Place close JNGFF3 pin 2,4



## Place close JNGFF3 pin 70,72,74

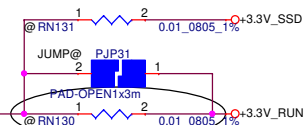


## 2280 SSD NGFF slot C Key M



+3.3V\_SSD from SSD storage protection power gate control

0212 change  
RN130 covering green printing for co-lay materials



2.8A

SSD\_SCP#\_R@RN1291 0 0.0201\_5%  
NVME\_LED# @RN100 0.0201\_5%  
SSD\_SCP# <58>

M2280\_DEVSLP <10>

PCH\_PLTRST#\_AND <11,38,42,52,70>  
CLKREQ\_PCIE#2 <11>  
PCIE\_WAKE# <42,52,59>

SUSCLK\_R@RN99 1 2 0.0201\_5%  
SUSCLK <11,52>

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M2 2280 Socket

LA-G871P

Date: Tuesday, March 05, 2019 Sheet 68 of 109


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# Reserve

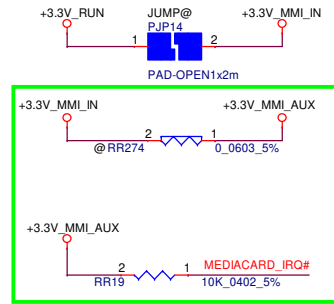
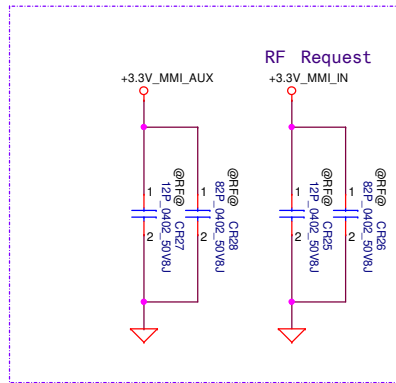
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		Compal Electronics, Inc.	
Title		eMMC / UFS	
Size	Document Number		Rev
	LA-G871P		1.0
Date:	Tuesday, March 05, 2019		Sheet 69 of 109

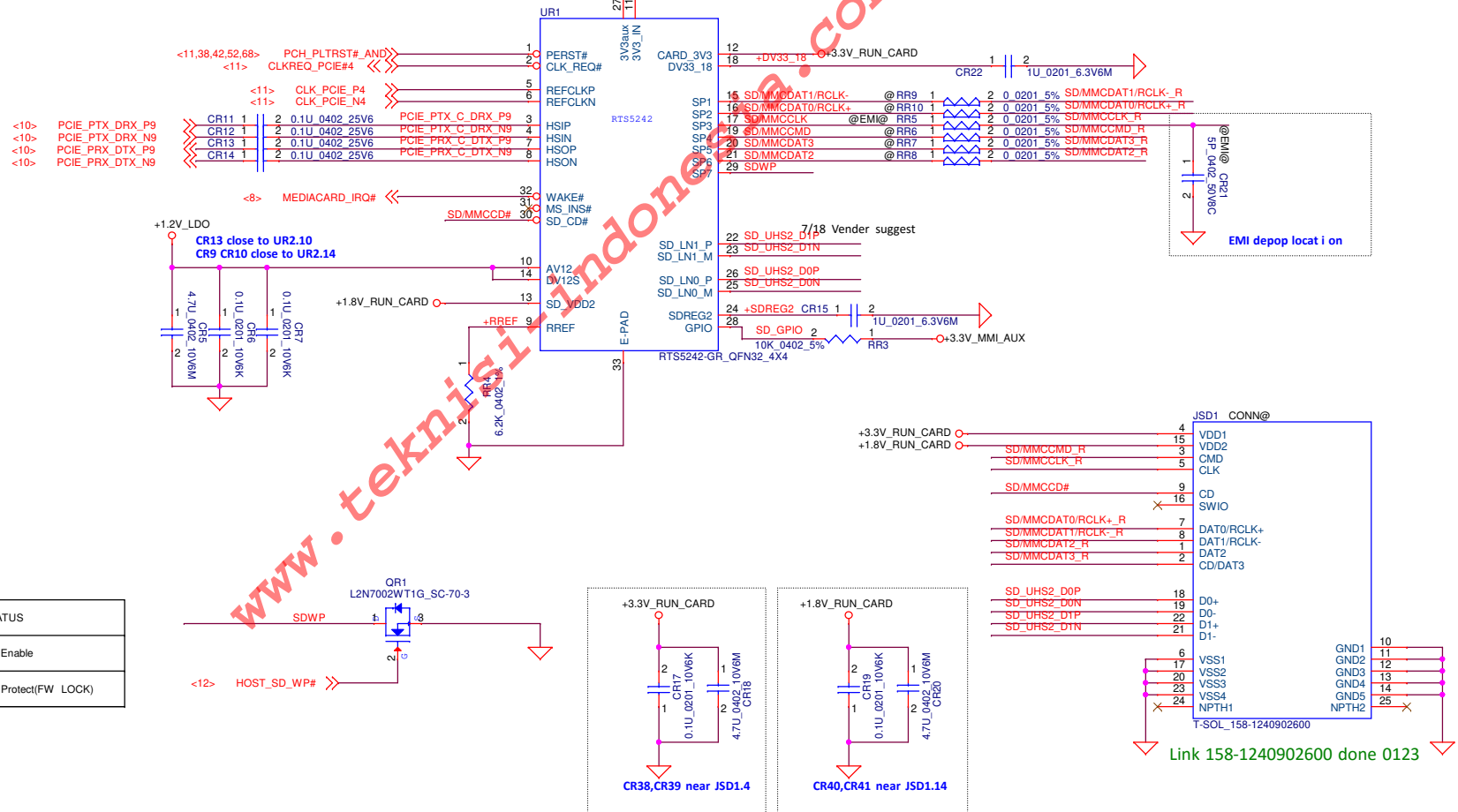
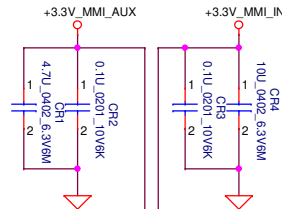
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# For PCIE Interface

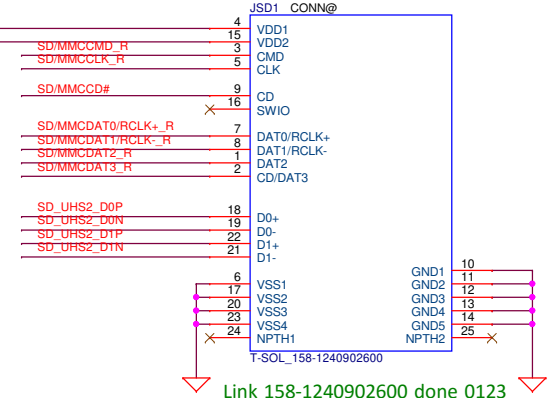
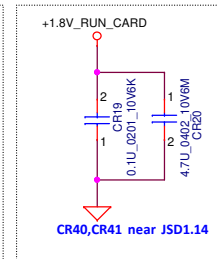
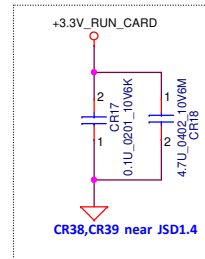
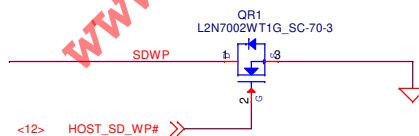


support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)

7/18 Vender suggest.



HOST_SD_WP#	SDWP	STATUS
High	Low	Write Enable
Low	High	Write Protect(FW LOCK)



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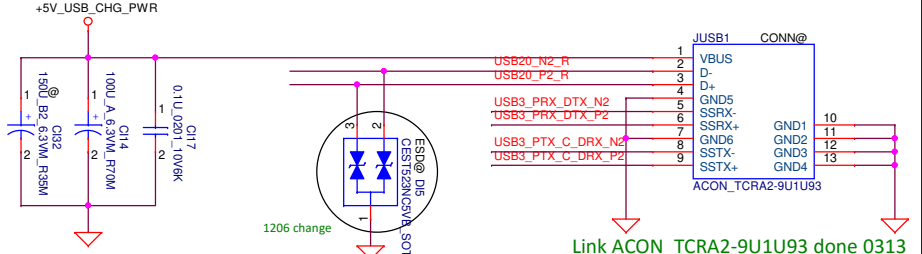
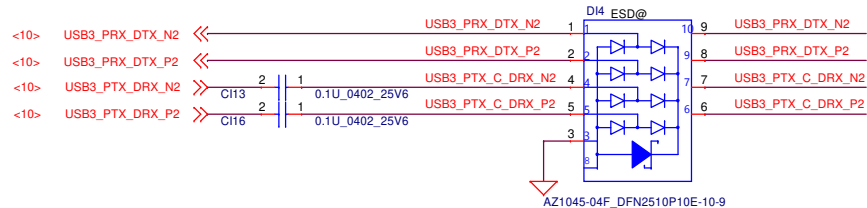
Card Reader RTS5242

LA-G871P

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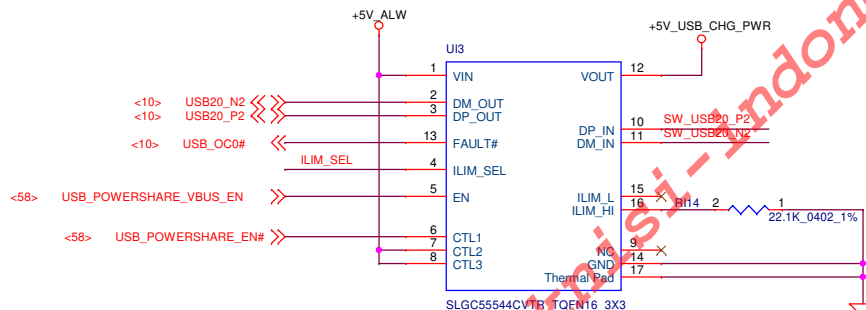
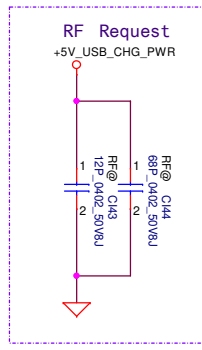
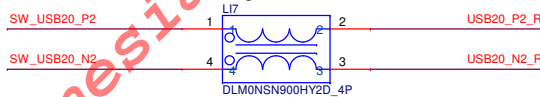
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For Merion 14

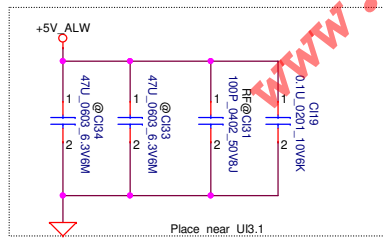
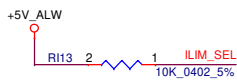


Merion Limit height  
DI5 change to H=0.9mm(MAX)

Merion14 swap LI7 net for layout routing



Link Seligro SA000097E10 Done  
MAIN:SLGC55544CVTR



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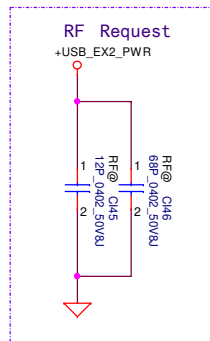
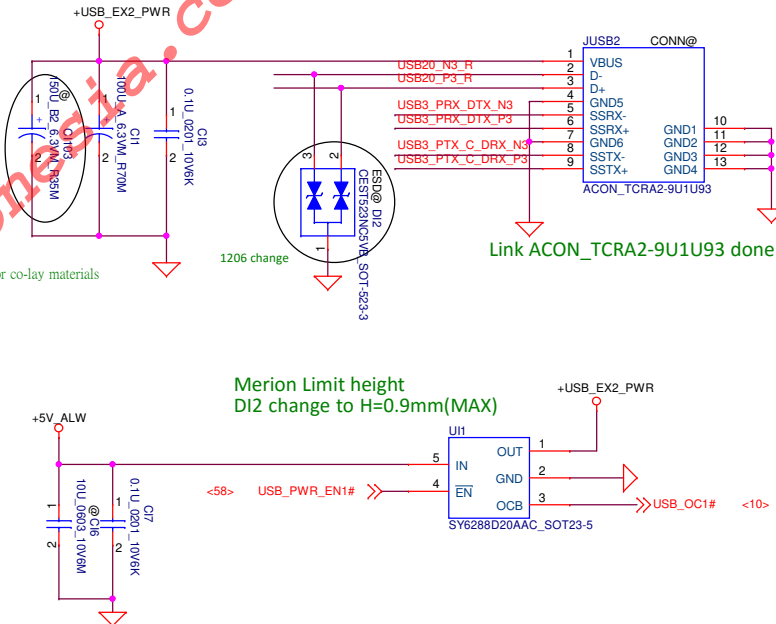
Title		JUSB1+PS
Size	Document Number	LA-G871P
Date:	Tuesday, March 05, 2019	Sheet 71 of 109

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**LA-G871P**

Rev	1.0
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Title		USB2/USB3 DB	
Size	Document Number		Rev
	LA-G871P		1.0
Date:	Tuesday, March 05, 2019		Sheet 73 of 109

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Title		Dock	
Size	Document Number	LA-G871P	Rev 1.0
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Reserve for USB		
Size	Document Number	Rev
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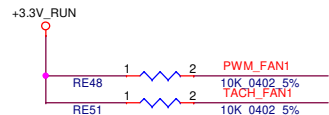
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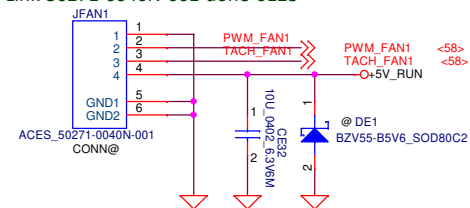
		
Compal Electronics, Inc.		
Title		
Reserve for USB		
Size	Document Number	Rev
	LA-G871P	1.0
Date:	Tuesday, March 05, 2019	Sheet 76 of 109

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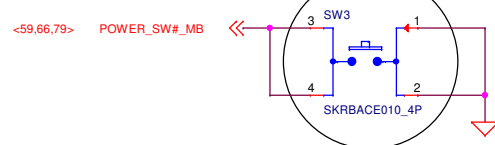


Link 50271-0040N-001 done 0123



Fan follow X9 project PIN DEFINE

## POWER & INSTANT ON SWITCH TOP

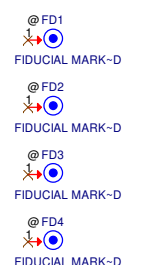


1213 change  
Update SW3 footprint

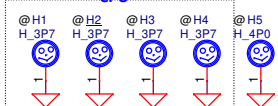
LED Circuit Control Table

	LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

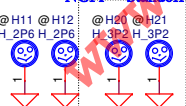
## Fiducial Mark



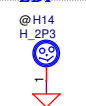
## CPU



## NGFF Standoff

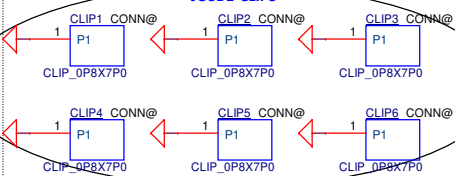


## EDP



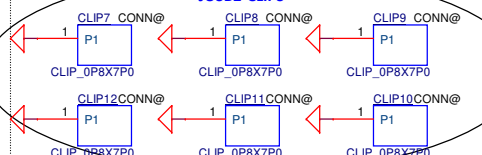
1213 change  
From CLIP\_OP6X7P0 to CLIP\_OP8X7P0

## JUSB1 CLIPS

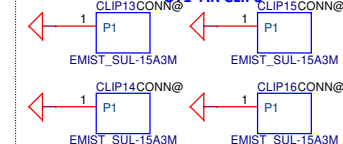


1213 change  
From CLIP\_OP6X7P0 to CLIP\_OP8X7P0

## JUSB2 CLIPS



## UT1 AR CLIPS



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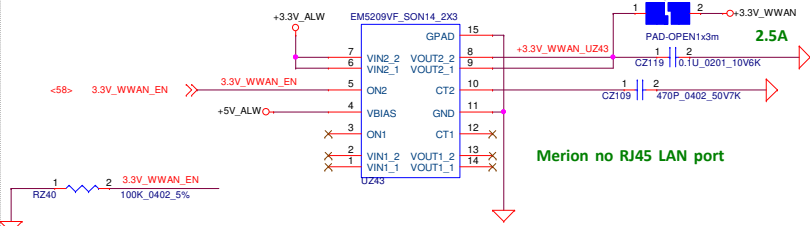
PWRBTN, PAD, ME, FAN

LA-G871P

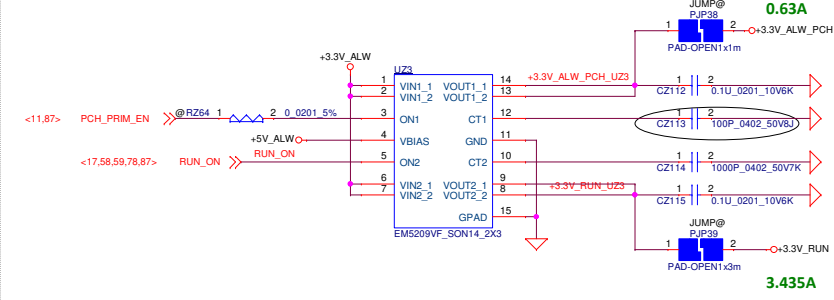
Date: Tuesday, March 05, 2019 Sheet 77 of 109

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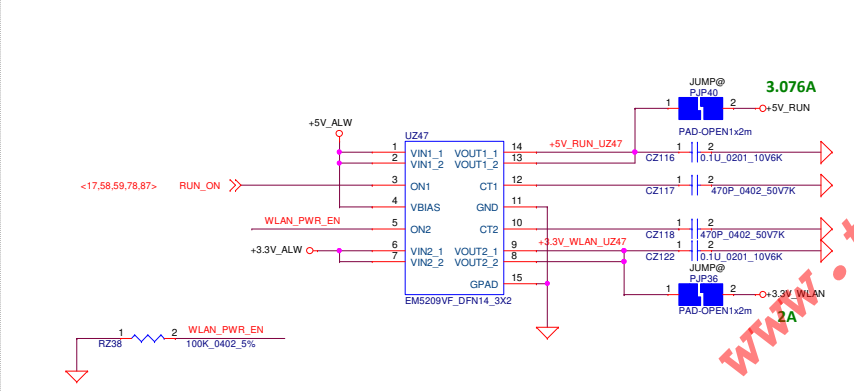
### +3.3V\_WWAN/+3.3V\_LAN source



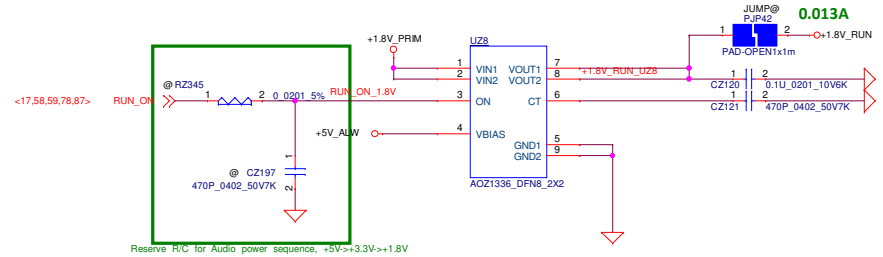
### +3.3V\_ALW\_PCH/+3.3V\_RUN source



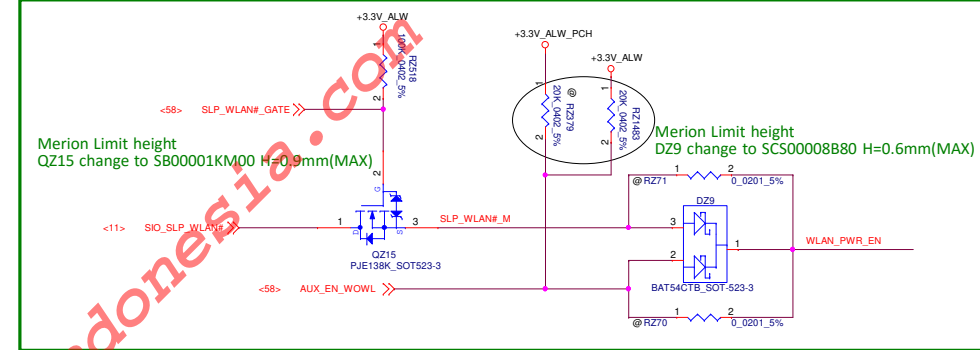
### +5V\_RUN/+3.3V\_WLAN source



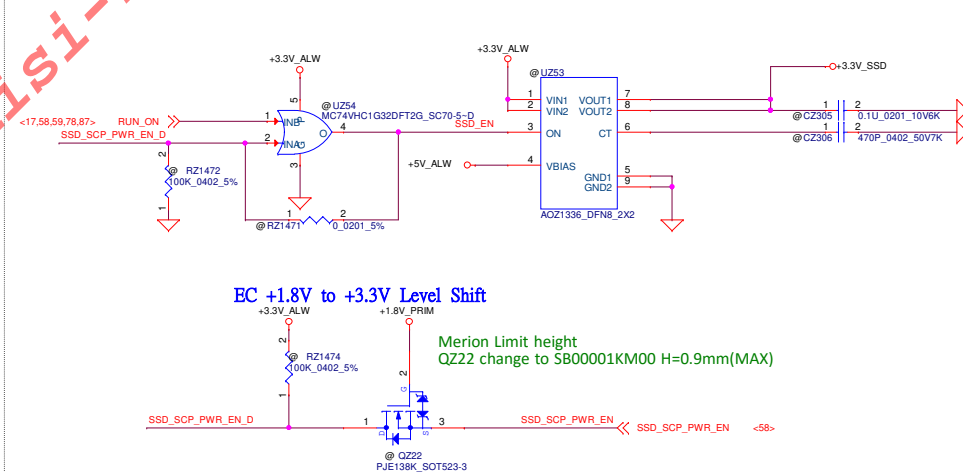
### +1.8V\_RUN source



EC request to reserve OR gate for WLAN power enable



Reserve for SSD storage protection power gate control Reference Berlinetta CFL pilot



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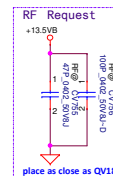
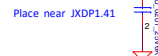
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Power control

LA-G871P

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The schematic shows the internal circuitry of the ME FWP PCH. It includes a +3.3V\_ALW\_PCH supply connected to a network of capacitors (C1, C2, C3) and resistors (R1, R2). A PTST pop RC222 and SW1 are connected to the ME\_FWP\_PCH pin. The circuit also features a 0212 Change component, a 1K\_0402\_5% resistor, and a 100nF capacitor. The output of the circuit is labeled <1>2</1>, which is connected to the ME\_FWP\_PCH pin. The circuit is powered by a 3.3V supply.

**ME FWP PCH has internal 20K PD -> Link SSAJ120100 done 0514**  
(suspend power rail)

**FLASH DESCRIPTOR SECURITY OVERRIDE**

- LOW = ENABLE (DEFAULT) -->Pin2 & Pin3 short
- HIGH = DISABLE (MC can update) -->Pin1 & Pin3 short

Date: Tuesday, March 05, 2019 Sheet 79 of 10

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Google Debug & INAs


LA-G871P

Date: Tuesday, March 05, 2019 Sheet 80 of 109 Rev 1.0

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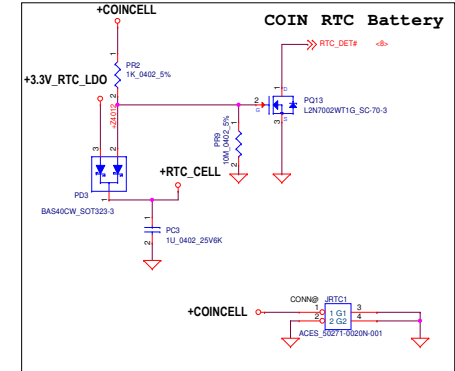
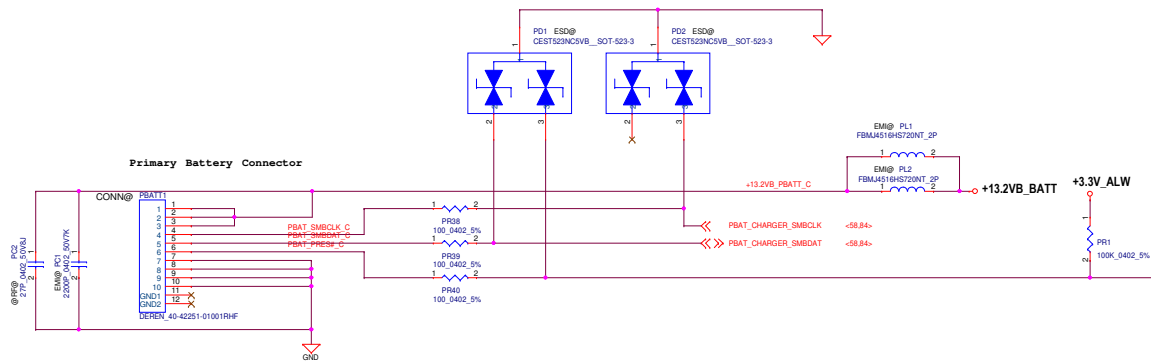
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Title		<b>PWR-Block Diagram</b>	
Size	Document Number	Rev	
	<b>LA-G871P</b>	<b>1.0</b>	
Date: Tuesday, March 05, 2019		Sheet	81 of 109

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		Compal Electronics, Inc.	
		Battery Connector/ RTC	
Doc	Document Name	LA-G871P	
Date	Issued	March 05, 2019	Sheet 83 of 109

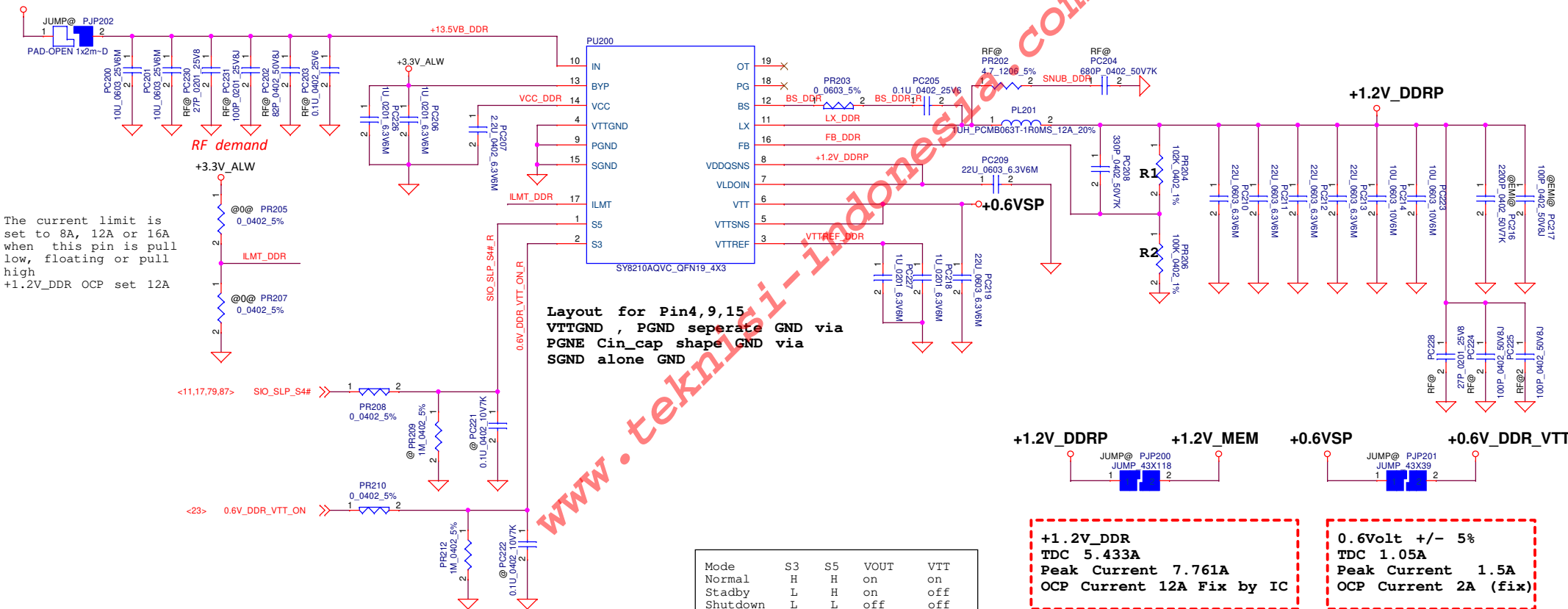
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+13.5VB



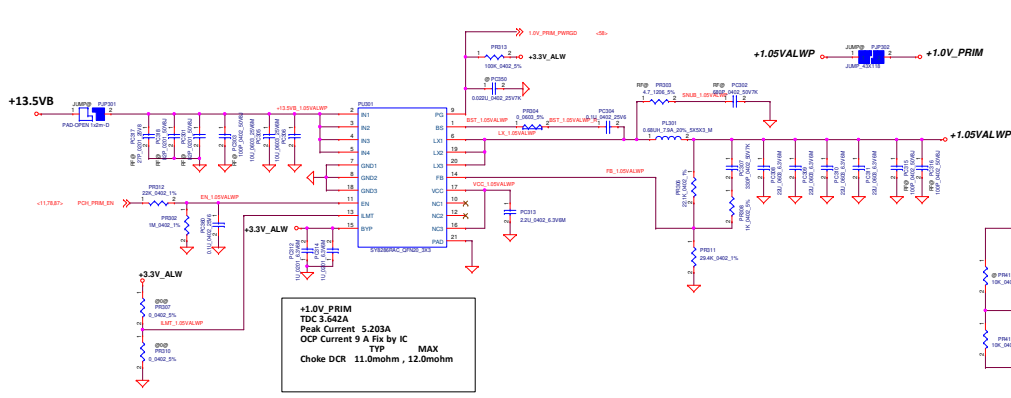
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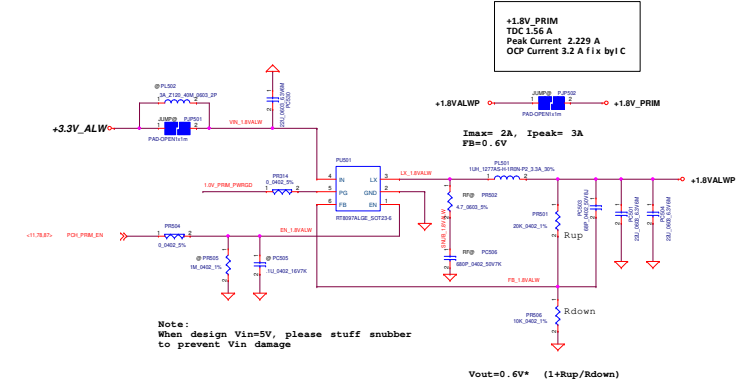
Compal Electronics, Inc.

Title			
+1.2V MEN/+0.6V DDR VTT			
Size	Document Number		Rev
	LA-G871P		1.0
Date:	Tuesday, March 05, 2019	Sheet 86 of 109	

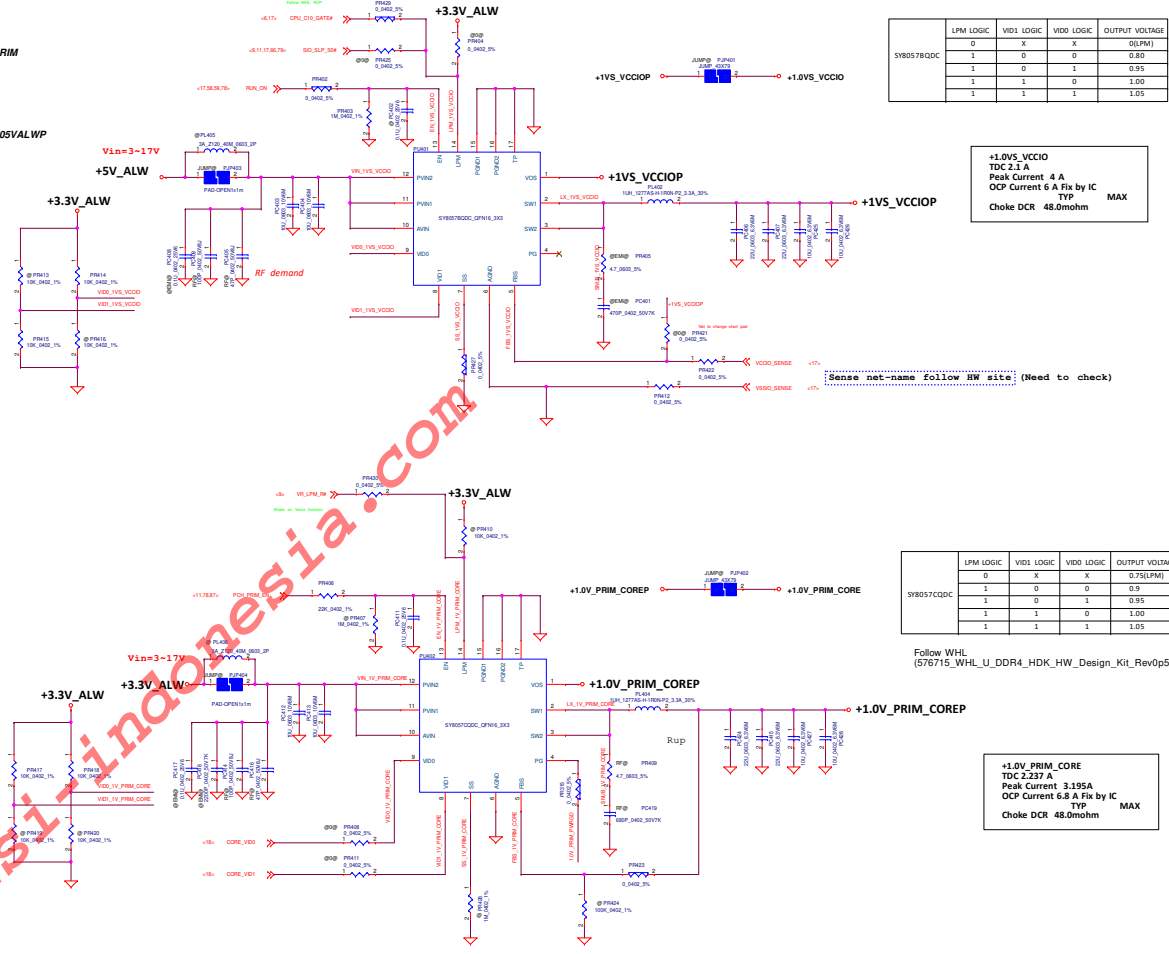
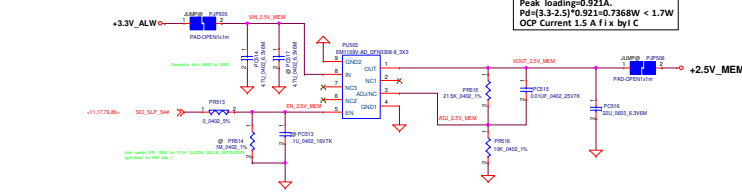
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The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high



**+2.5V MEM**  
TDC 0.645A by power budget  
AP7361 U-DNR0300-8 f<sub>ld</sub> limit=1.7W  
Peak loading=0.921A  
P<sub>ld</sub>=(3.3-2.5)\*0.921=0.736W < 1.7W  
OCP Current 1.5 A fix by IC



LPM LOGIC	VDD1 LOGIC	VDD0 LOGIC	OUTPUT VOLTAGE
0	X	X	0.95V
1	0	0	0.95
1	0	1	0.95
1	1	0	1.00
1	1	1	1.05

LPM LOGIC	VDD1 LOGIC	VDD0 LOGIC	OUTPUT VOLTAGE
0	X	X	0.75V(LPM)
1	0	0	0.9
1	0	1	0.95
1	1	0	1.00
1	1	1	1.05

Follow WHL (S76715\_WHL\_U\_DDR4\_HDK\_HW\_Design\_Kit\_Rev0p5)

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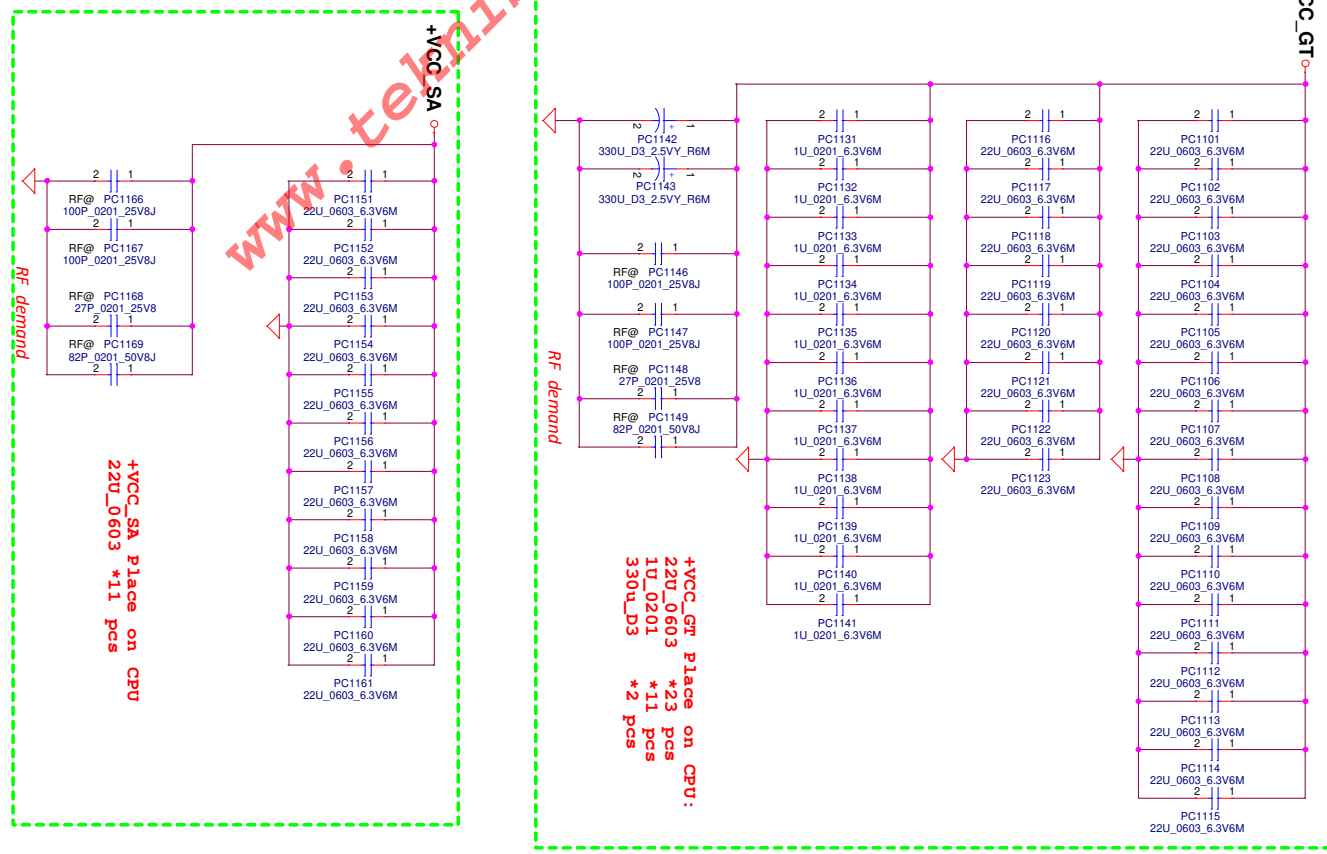
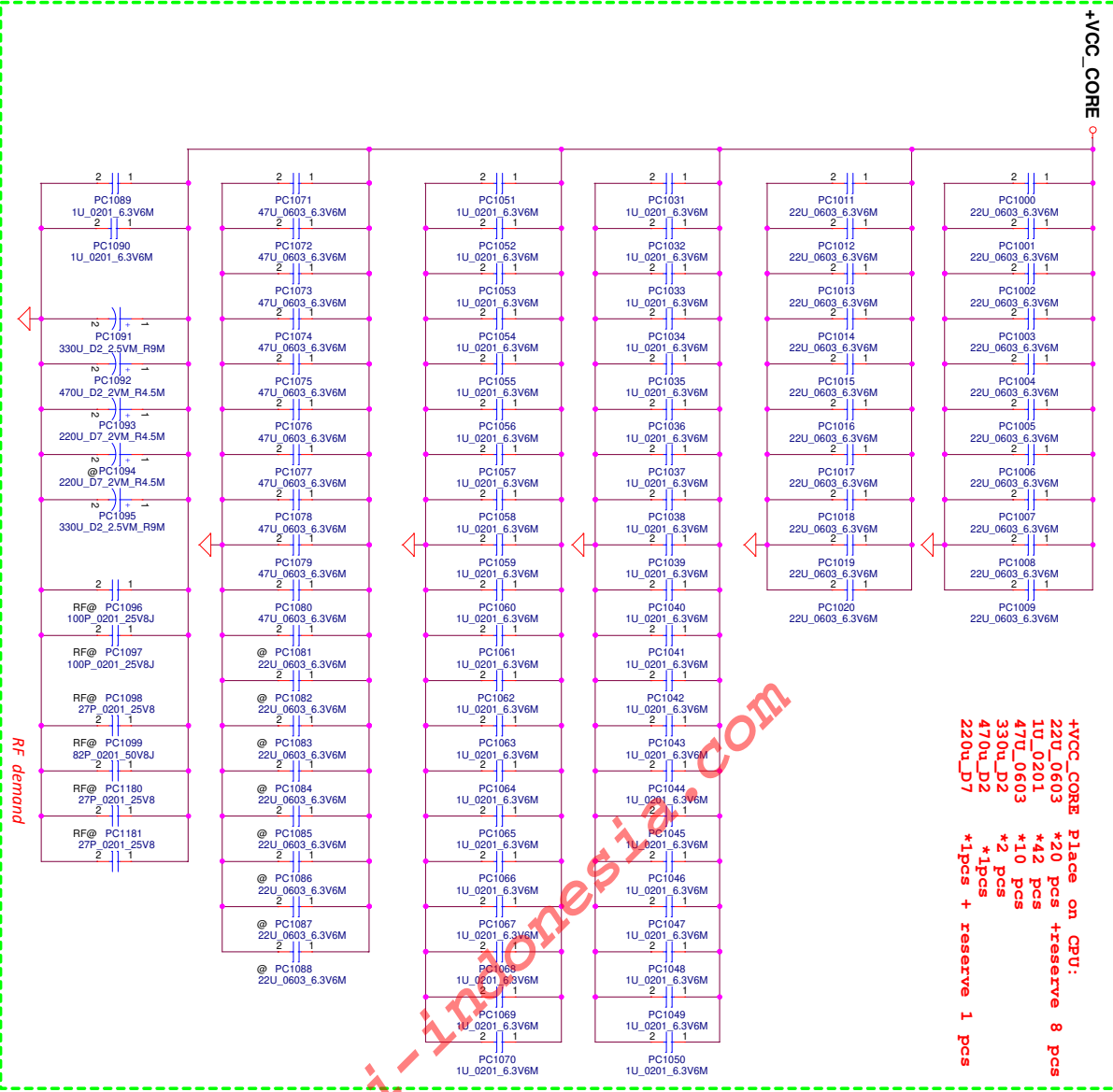
**+1VALWP/VCCIO/PRIM CORE/1.8V/2.5V**

LA-G871P

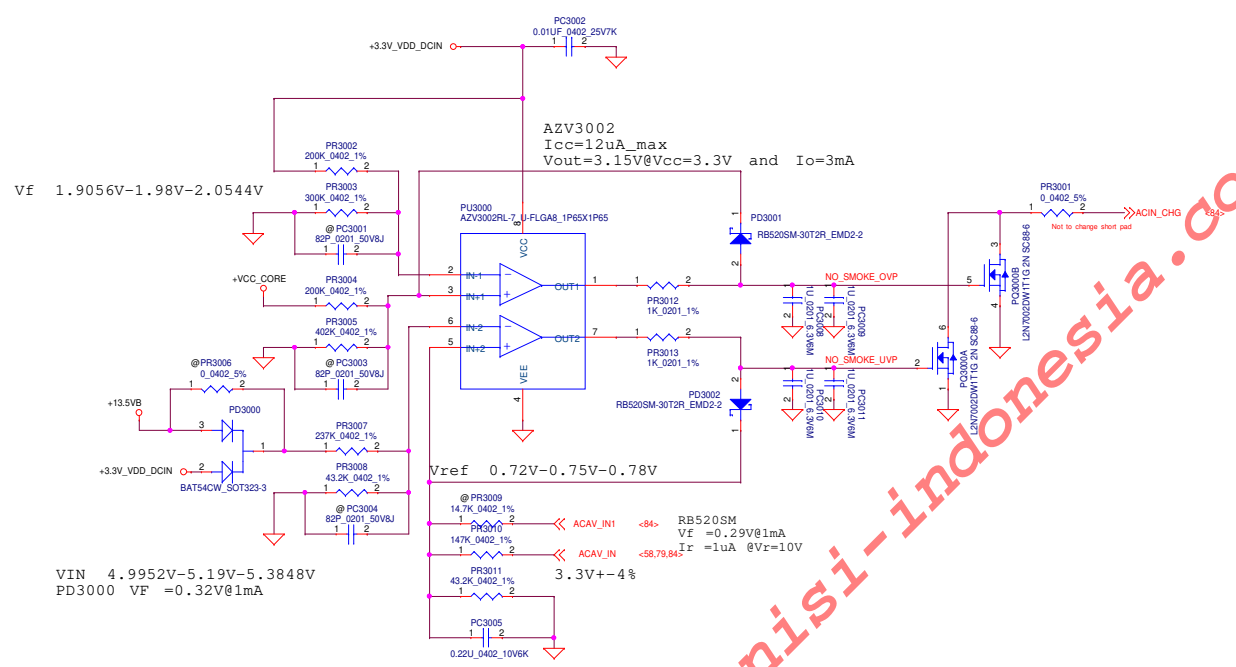
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Charger UVP/VCORE OVP			
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


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## U42


PC626 U42@  0.1U_0402_25V6	PR613 U42@  97.6K_0402_1%	PR621 U42@  316_0402_1%	PC624 U42@  0.022U_0402_16V7K
PR638 U42@  523_0402_1%	PR622 U42@  2.49K_0402_1%	PC616 U42@  68P_0402_50V8J	PC617 U42@  1200P_0402_50V7K

## U22

PC626 U22@  0.047U_0402_25V7K	PR613 U22@  84.5K_0402_1%	PR621 U22@  316_0402_1%	PC624 U22@  0.033U_0402_25V7K
PR638 U22@  422_0402_1%	PR622 U22@  1.65K_0402_1%	PC616 U22@  33P_0402_50V8K	PC617 U22@  1200P_0402_50V7K

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Version Change List ( P. I. R. List )					
Item	Page #	Date	Issue Description	Solution Description	Rev.
19	P088 P089	08/22	CPU VR input Low noise MLCC PCB footprint update : C_0603-S3	IA input : PC658 / PC657 / PC656 / PC682 / PC683 / PC684 / PC672 / PC673 GT input : PC675 / PC674 / PC664 / PC665 SA input : PC612 / PC608 IA output : PC1071 / PC1072 / PC1073 / PC1074 / PC1075/ PC1076 / PC1077 / PC1078 / PC1079 / PC1080	X01
20	P090	08/22	Un-stuffed CPU +VCC_CORE output MLCC change value	Change reserve location from 47uF to 22uF (Keep un-stuff) PC1081 / PC1082 / PC1083 / PC1084 / PC1085 / PC1086 / PC1087 / PC1088	X01
21	P089	08/22	Remove double net name	Remove PU610 / PU612 / PU613 Dr.MOS pin 15(PVCC) double net name	X01
22	P087	08/23	Change PU301, PU501 powergood connection netname	Change connection to 1.0V_PRIM_PWRGD from 1.8V_PRIM_PWRGD (PU301, PU501)	X01
23	P087	08/28	R/C for WHL sequence	1. Add PR313 : 100K_0402_5% 2. Add PR314 / PR315 : 0 ohm ( 3. Reserve PC350 footprint to PG (1.0V_PRIM_PWRGD) signal	X01
24	P089	08/28	1 barrel / 1 Type-C change solution 2	Change to Stuff : PR46 / PR41 / PR858 / PR857 / PQ12 / PR49 / PQ814 / PR861 Un-stuff : PR856 / PR43	X01
25	P091	09/04	Disable Charger UVP & VCORE OVP function	Un-stuff PR3001 for disable No Smoke function	X01
26	P090	09/14	DCIN AC detect tune value	Change PR817 to SD034249280 (S RES 1/16W 24.9K +-1% 0402)	X01
27	All	09/11	Follow schematic naming rule	Jump BOM structure change Solder -> JUMP@ Not Solder -> @JUMP@	X01
1	P091	11/05	Charger UVP/VCORE OVP circuit	1. PR3002 change to 200K_0402_1% (SD034200380) 2. PR3003 change to 300K_0402_1% (SD034300380) 3. PR3001 change to stuff 4. Add PC3008 / PC3009 on NO_SMOKE_OVP 5. Add PC3010 / PC3011 on NO_SMOKE_UVP	X02
2	P084 P088	11/05	Charger IC PU700 & CPU Controller IC PU602 change P/N for MP	1. PU700 change P/N to SA0000BWG0L for MP 2. PU602 change P/N to SA0000BYJ0L for MP	X02
3	P090	11/05	Barrel & typeC B2B MOSFET P/N change	1. Check PQ4/PQ801/PQ702 1st parts is SB00001MT00 (SB00001MT00 - AONR21357 1P DFN3X3-8) . 2. PQ9 / PQ800 CPN change to SB00001BX1L (EMZB08P03V 1P EDFN3X3-8)	X02
4	All	11/28	0 ohm short pad total 69 pcs	PR19, PR20, PR22, PR25, PR861, PR42, PR44, PR46, PR47, PR49, PR100, PR104, PR105, PR111, PR119, PR120, PR203, PR208, PR210, PR304, PR314, PR315, PR402, PR423, PR504, PR513, PR602, PR603, PR606, PR614, PR616, PR620, PR625, PR659, PR662, PR664, PR679, PR687, PR709, PR713, PR715, PR719, PR721, PR722, PR727, PR729, PR731, PR736, PR737, PR740, PR741, PR743, PR814, PR816, PR818, PR820, PR826, PR827, PR829, PR834, PR836, PR840, PR844, PR853, PR854, PR858, PR859, PR671, PR692	X02
5	P082	11/28	Barrel & typeC B2B control circuit	Change to un-stuff parts : PC13 / PU3 / PR45 / PC814 / PU801 / PR855	X02
6	P084 P089	12/03	Add " -NPM " PCB Footprint to cover green paint for Co-lay Depop Component.	PJP700 -> JUMP_43X118-NPM PL602 -> 9A_280_1812_2P-NPM	X02
7	P082	12/04	ESD Request	PD1, PD2 change P/N to SCA00004700, S ZEN ROW CEST523NC5VB 3P C/A SOT-523 AU Due to AMZ SCA00002X00 has be removed in ESD common pool	X02
8	P082	12/12	PD803 voltage derating back up solution	1. Remove PR868 reserve 0ohm 2. Add PR892 / PR893 for PD803 voltage derating back up solution. SD002220A80 - S RES 1/8W 22 +-5% 0805 3. PD803 Pin 1 add net name : +20V_LDO_INPUT	X02
9	P084	12/13	Charger input current sense R for more quickly sensing	PR701 / PR702 change to 1_0603_1% (SD014100B80) for more quickly sensing	X02
10	P091	12/13	Charger UVP/VCORE OVP circuit	1. PR3010 change value from 14.7K to 147K(SD034147380) for more sequence margin. 2. PR3011 change value from 4.32K to 43.2K(SD034432280) for more sequence margin.	X02
11	P085 P086	12/13	RF Request	Add PC228 27pF on +1.2VDDRP, PC142 27pF on +5V_ALWP for RF demand	X02
12	P087	12/28	+1.0VS_VCCIO change from local sense to remote sense	1. PR421 change to depop (@08) 2. PR412, PR422 change to pop	X02
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NVPRO@ RC734  
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NVPRO@ RC571  
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NVPRO@ RC572  
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NVPRO@ RC33  
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NVPRO@ UC5  
GD25B64CYIGR

NVPRO@ RC25  
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NVPRO@ BZ59  
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Version Change List ( P. I. R. List )			Issue	Solution	
Item	Page#	Date	Description	Description	Rev.
1	All	2018/07/23	Updated page define according to Dell request	Updated page define according to Dell request.	0.2 (X01)
2	79	2018/07/23	1.Modified QZ3 footprint to correct 2.Modified parts pin define to correct	1.Change QZ3 footprint to SOT-323 from SOT-23. 2.Change SW1 pin define.	0.2 (X01)
3	09	2018/07/23	Modified parts pin define to correct	Change JASA1 pin define (swap pin1&4, pin2&3).	0.2 (X01)
4	44	2018/07/23	1.Modified parts location to align with X9 2.Change PD controller to 65982DD	1.Change CT358 location to CT82. 2.Change UT5 part to SA0000C800 from SA0000BIJ00.	0.2 (X01)
5	11	2018/07/23	RTC elapsed time can not meet the Spec (spec: +/- 2 secs)	Change CC23, CC26 part to 15P_0402_50V8J from 12P_0402_50V8J.	0.2 (X01)
6	50	2018/07/23	1.Modified parts BOM Structure 2.Modified layout Limit height problem	1.Change RC24 BOM Structure to @NVPRO from @. 2.Change QC2 part to SB000014X00 from SB00000PV00.	0.2 (X01)
7	52	2018/07/23	Modified parts pin define to correct	Change JANT1, JANT2 pin define (swap pin1&5, pin2&4).	0.2 (X01)
8	102	2018/07/23	Modified NVPRO BOM option RZ58~RZ60 to correct	Change RZ58~RZ60 BOM option part to 33_0402_1% from 33_0201_1%.	0.2 (X01)
9	56	2018/07/23	Modified according to ESD request	Change DA2 part to SCA00001A00 from SC600001600.	0.2 (X01)
10	66	2018/07/23	1.Modified layout Limit height problem 2.Change ST TPM to ST33HTPH2032AHC1 (MP version) 3.Add FPR_RST# pull high, align with merion13	1.Change DZ11 part to SCA00002A00 from SCA00001B00. 2.Change UZ12 part to SA0000C5G10 from SA00009SO40. 3.Add RZ1392 (100K_0201_5%) pull high to +3.3V_FPBTN.	0.2 (X01)
11	59	2018/07/23	Modified layout Limit height problem	Change UE4 part to SA00007YE00 from SA00007WE00.	0.2 (X01)
12	78	2018/07/23	Modified layout Limit height problem	Change DZ9 part to SCS00008B80 from SCS00006400. Change QZ15, QZ22 part to SB00001KM00 from SB00000VD00.	0.2 (X01)
13	14	2018/07/23	Modified layout Limit height problem	Change QC4 part to SB000014X00 from SB00000PV00.	0.2 (X01)
14	38	2018/07/23	Modified layout Limit height problem	Change QV2, QV7 part to SB00000NK00 from SB00000UO00.	0.2 (X01)
15	40	2018/08/09	1.Modified layout Limit height problem 2.Modified parts according to EMI & EE test result	1.Change QV4, QV5 part to SB00000NK00 from SB00000UO00. 2.Change RV26, RV29, RV32, RV35 part to 130_0402_5% from 300_0402_5%. Change LV31~38 to 5.6_0402_5% from SHI00006Q00. Change LV31~38 location to RV56~RV63.	0.2 (X01)
16	79	2018/08/09	1.Dell request to modify M_BIST circuit 2.Modified parts to correct capacitance voltage 3.Delete unnecessary parts, align with X10 projects	1.Change netname to M_BIST from M_BITS. Change RZ1413 part to SD028330380 (330K_0201_5%) from SD00000HX80 (221K_0201_1%). Add location RZ1482 (1M_0402_5%) pull up to +3.3V_ALW. Change RZ1413, DZ12 to depop from pop. 2.Change CZ218 part to SE00000UC00 (1U_0201_6.3V6M) from SE000013500 (1U_0201_10V6M). 3.Delete location RV632 (0_0402_5%).	0.2 (X01)
17	18	2018/08/09	1.Modified parts downsize according to Intel confirmed 2.Modified parts according to Intel BSOD issue recommend 3.Reserved WHEA circuit 4.Reserved WHEA R/C Filter circuit	1.Change CC65, CC66, CC73, CC75, CC98, CC1463, CC1464, CC67, CC80, CC83 part to SE00000UC00 (1U_0201_6.3V6M) from SE00000K80 (1U_0402_6.3V6K). Add location CC68, CC69, CC70 (1U_0201_6.3V6M). Change CC72 part to SE000000580 (0.1U_0201_6.3V6K) from SE095104K80 (0.1U_0402_10V6K). Delete location CC74 (0.1U_0402_10V6K). 2.Change LC1~LC3 part to SHI0000XL00 (2.2uH 0603 INDUC) from SM01000RR00 (0603 Bead). Change CC100, CC102 part to SE00000M000 (22U_0603_6.3V6M) from SE00001500 (47U_0603_6.3V6M). Add location CC103, CC104 (22U_0603_6.3V6M). Change LC2, LC3, CC100, CC102 to pop from depop. Change RC173, RC175 to depop from pop. 3.Delete location RC846 (0_0201_5%). Change CC85, CC86 part to SE00000M000 (22U_0603_6.3V6M) from SE000007280 (2.2P_0201_25V). Change LC1 BOM Structure to @ from @RF@. Change CC85, CC86 BOM Structure to @ from RF@. 4.Add location RC864 (0_0603_5%).	0.2 (X01)
18	58	2018/08/09	1.Modified according to GPIO map v1.4 2.Modified parts to correct capacitance voltage	1.Change netname to VCI_IN3# from NFC_ACTIVITY_STATUS#. Change netname to PTP_DISABLE# from TP_DISABLE#. 2.Change CE14, CE30, CE31, CE63 part to SE00000UC00 (1U_0201_6.3V6M) from SE000013500 (1U_0201_10V6M).	0.2 (X01)
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40	24	2018/08/22	Modified parts according to ESD request	Add location DD1(SCA00002A00).	0.2 (X01)	
41	70	2018/08/22	Modified parts to correct capacitance voltage	Change CR15,CR22 part to SE00000UC00(1U_0201_6.3V6M) from SE000013500(1U_0201_10V6M).	0.2 (X01)	
42	58	2018/08/22	Add RTC(coin battery) voltage detect circuit	Delete location T143 test point. Change EC side GPIO011 pin netname to RTC_DET# from GPIO011. Add offpage RTC_DET#.	0.2 (X01)	
43	58	2018/08/23	1.Fixed power sequence EA request 2.Modified RTC(coin battery) voltage detect circuit	1.Change RE361 pin 2 net connection to 1.0V_PRIM_PWRGD from 1.8V_PRIM_PWRGD. 2.Add location RE401 SD043100280(10K_0201_5%) pull up to +1.8V_PRIM_VTR3.	0.2 (X01)	
44	70	2018/08/23	Fixed double net problem	Delete net SDWP_Q.	0.2 (X01)	
45	78	2018/08/23	Fixed double net problem	Delete net +3.3V_SSD_UZ53.	0.2 (X01)	
46	01	2018/08/23	Add Motherboard DPN(PWB)	Add Merion14 PWB DD1CY.	0.2 (X01)	
47	66	2018/08/24	Modified parts according to ESD request	Add location DZ14,DZ15(SC300001Y00)	0.2 (X01)	
48	66	2018/08/27	1.Delete Semi-circular screw hole 2.Delete unnecessary screw hole	1.Delete location H26,H7,H6,H25,H9,H24,H23,H22. 2.Delete location H19.	0.2 (X01)	
49	38	2018/08/27	Update EDP connector symbol	Update JEDP1 connector symbol.	0.2 (X01)	
50	52	2018/08/27	Update 4x4 Antenna connectors symbol	Update JANT1,JANT2 connectors symbol.	0.2 (X01)	
51	52	2018/08/27	Modified JSPK1 pin define to correct routing	Swap JSPK1 pin define(1 to 8,2 to 7...).	0.2 (X01)	
52	58	2018/08/28	Modified SSD_SCP# pull up to reserved	Change location RE821 to depop from pop.	0.2 (X01)	
53	78	2018/08/31	1.Fixed power sequence EA request 2.Modified WLAN_PWR_EN pull up power rail according to Intel recommend 3.Delete unnecessary parts, align with X10 projects	1.Change CZ113 part to SE071101J80(100P_0402_50V8J) from SE074471K80(470P_0402_50V7K). 2.Add location RZ1483 SD028200280(20K_0402_5%) pull up to +3.3V_ALW. Change RZ379 to depop from pop. 3.Delete reserved location RZ375(20K_0402_5%).	0.2 (X01)	
54	01	2018/08/31	Modified Motherboard DPN(PWB) according to PJE request	Change Merion14 PWB to 7YM2P from DD1CY.	0.2 (X01)	
55	68	2018/08/31	1.Modified M.2 2280 Power Decoupling for support Intel Teton Glacier 2.Delete unnecessary parts, align with X10 projects	1.Change CN61,CN62 part to SE102104K0(0.1U_0402_10V7K) from SE00000SV00(0.1U_0201_10V6K). Add location CN79,CN80,CN81,CN82,CN84 SE076103K80(0.01U_0402_16V7K). Add location CN86 SE102104K00(0.1U_0402_10V7K). Add location CN87 SE00000M000(22U_0603_6.3V6M). 2.Delete location RN125~RN128,RN77,RN78,RN81,RN82(0_0201_5%).	0.2 (X01)	
56	79	2018/08/31	Delete unnecessary parts, align with X10 projects	Delete reserved location RE375(0_0201_5%). Delete location RE560(0_0201_5%).	0.2 (X01)	
57	11	2018/08/31	Delete unnecessary parts, align with X10 projects	Delete location RC740(0_0201_5%). Delete net PCH_PLTRST#_EC.	0.2 (X01)	
58	66	2018/08/31	Delete unnecessary parts, align with X10 projects	Delete location RZ87(0_0201_5%). Delete reserved location DZ7(SCS00006300). Change RZ1473 to depop from pop.	0.2 (X01)	
59	56	2018/08/31	Modified location to correct	Change location CA78 to CA29. Change location CA79 to CA49.	0.2 (X01)	
60	52	2018/09/03	JSIM1 footprint change to use 2nd source footprint	Change JSIM1 footprint to TAISO_159-1000300600 from JAE_SF51S006V4DR1000Q.	0.2 (X01)	
61	09	2018/09/04	Modified CNV_RGI_DT pull up follow Intel RVP	Change RC842 part to SD028200280(20K_0402_5%) from SD028100280(10K_0402_5%).	0.2 (X01)	
62	08	2018/09/04	Modified GPP_C2 pull up follow Intel RVP	Change RC266 part to SD028470180(4.7K_0402_5%) from SD028220180(2.2K_0402_5%).	0.2 (X01)	
63	38	2018/09/05	Reserved FUSE package location	Change RZ1387,RV100 to SD00000ZS00(0.01_0603_1%) from SD00000XJ00(0.01_0805_1%). Add location RZ98,RV103 SD00000ZS00(0.01_0603_1%).(footprint is FUSE SP040007G00)	0.2 (X01)	
64	58	2018/09/07	Modified FPR pull up power rail	Change RE706~RE709 pull up power rail to +3.3V_FPBTN from +3.3V_RUN.	0.2 (X01)	
65	38	2018/09/11	Modified part according to sourcer request	Change CV15 part to SE00000G880(0.1U_0402_25V6) from SE074104K80(0.1U_0402_50V7K).	0.2 (X01)	
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Version Change List ( P. I. R. List )			Issue	Solution		Rev.
Item	Page#	Date	Description	Description		
66	79	2018/10/31	1.Modified M-BIST circuit for DC mode LED flash issue 2.Modified part according to sourcer request	1.Change CZ218 part to SE00000X880(2.2U_0201_6.3V6M) from SE00000UC00(1U_0201_6.3V6M) 2.Chane CZ218 part to SE000008880(2.2U_0402_6.3V6M) from SE00000X880(2.2U_0201_6.3V6M)	0.3 (X02)	
67	56	2018/10/31	Modified part according to sourcer request	Chane CA35 part to SE000008880(2.2U_0402_6.3V6M) from SE00000X880(2.2U_0201_6.3V6M)	0.3 (X02)	
68	59	2018/10/31	1.Modified part according to sourcer request 2.Modified Board ID resistor to X02	1.Chane CE12 part to SE000008880(2.2U_0402_6.3V6M) from SE00000X880(2.2U_0201_6.3V6M) 2.Change RE79 part to SD028620280(62K_0402_5%) from SD028130380(130K_0402_5%)	0.3 (X02)	
69	38	2018/10/31	1.Add Fuse part,modified location 2.Modified part to reserved Fuse location 3.Modified CAM,Touch Fuse	1.Change location RV100 to FV1,RV103 to FV2,RZ98 to FZ1,RZ1387 to FZ2. Change RV100,RV103,RZ98,RZ1387 part to SP040007G00(Fuse 1A_0603) 2.Change RZ1476 part to SD013000080(0_0603_5%) from SD028000080(0_0402_5%) 3.Change FZ1,FV2 part to SP040007F00(Fuse 0.5A_0603) from SP040007G00(Fuse 1A_0603)	0.3 (X02)	
70	18	2018/10/31	Modified CPU BV23 pin power rail follow Intel RVP	Change CPU BV23 pin power rail to +3.3V_ALW_PCH from +3.3V_SPI	0.3 (X02)	
71	66	2018/10/31	Modified parts align with X10 projects	Change RZ10(100K_0402_5%) to pop from depop. Change RZ1414(0_0201_5%) to depop from pop	0.3 (X02)	
72	58	2018/10/31	Modified RTC_DET# net connection to PCH from EC side	Change RTC_DET# net connection to PCH side(GPP_D3) from EC side(GPIO011). Delete location RE401 pull up SD043100280(10K_0201_5%)	0.3 (X02)	
73	08	2018/10/31	Modified RTC_DET# net connection to PCH from EC side	Change RTC_DET# net connection to PCH side(GPP_D3) from EC side(GPIO011). Add location RC866 pull up SD043100280(10K_0201_5%)	0.3 (X02)	
74	64	2018/10/31	Modified part follow LED light test result	Change RZ32 to SD028100180(1K_0402_5%) from SD028330080(330_0402_5%)	0.3 (X02)	
75	52	2018/11/30	1.Modified parts shortage problem 2.Modified part according to RF request 3.Modified layout Limit height problem	1.Change QZ17 from SB00001GC00 to SB00001KM00 2.Change RZ1460(0_0201_5%) and RZ1461(0_0201_5%) from depop to pop 3.Change part CZ26 from SGA00005T00(H.max=1.9mm) to SGA00006800(H.max=1.1mm)	0.3 (X02)	
76	11	2018/12/06	Follow NB14 UU AR, follow Intel CNVi recommendation	Change RC237(100k_0402_5%) from depop to pop	0.3 (X02)	
77	52	2018/12/06	Follow NB14 UU AR, follow Intel CNVi recommendation	1.Add RZ603 CNV_BRI_PTX_DRX_R pull up(10k_0402_5%) to +1.8_PRIM for reserve 2.Delete location RZ371(0_0201_5%) and RZ81(0_0201_5%)	0.3 (X02)	
78	12	2018/12/06	Follow NB14 UU AR, follow Intel CNVi recommendation	1.Change RC752 from SD028750280(75k_0402_5%) to SD034715280(71.5k_0402_1%) 2.Change RC640 from SD034715280(71.5k_0402_1%) to SD028750280(75k_0402_5%)	0.3 (X02)	
79	13	2018/12/06	Follow NB14 UU AR, follow Intel CNVi recommendation	UC1_CR35 add test point(T423)	0.3 (X02)	
80	11	2018/12/11	Intel CNVi recommendation RC237 pop,But cold reset and global reset sequence timing fail,So depop RC237	Change RC237(100k_0402_5%) from pop to depop	0.3 (X02)	
81	52	2018/12/11	Add 4X4 WWAN netname	Add netname +2.7V_ANT_R connect to JNGFF2.20, +1.8v_ANT_R connect to JNGFF2.24	0.3 (X02)	
82	72	2018/12/11	Add CAP for reserve material shortage problem	Add CI103(150U_B2_6.3VM_R35M) reserve Co-layer with CI1(100U_A_6.3VM_R70M) material shortage problem	0.3 (X02)	
83	77	2018/12/13	Modified according to DFX request	Change CLIP1~CLIP12 form CLIP_0P6X7P0 to CLIP_0P8X7P0	0.3 (X02)	
84	52	2018/12/13	Modified according to RF request	1.Change CZ206 and CZ207 from depop to pop and change value from 100P to 27P 2.Add CZ311 and CZ312(27P_0402_50V8J) on +3.3V_WWAN for RF request	0.3 (X02)	
85	38	2018/12/13	Modified according to RF request	1.Add CZ313(27P_0201_25V8) on +LCDVDD for RF request 2.Add CZ314(27P_0402_50V8J) on +BL_PWR_SRC for RF request	0.3 (X02)	
86	64	2018/12/13	Modified according ME request	Change RZ28 from SD028330080(330_0402_5%) to SD028150080(150_0402_5%)	0.3 (X02)	
87	38	2018/12/17	Modified location to correct	1.Change Location from CZ313 to CV757 2.Change Location from CZ314 to CV758	0.3 (X02)	
88	9	2018/12/18	Reserve for MOV issue	Add RC867(0_0201_5%) reserve for BITS392123, can't play music after resume from CMS with headphone connected	0.3 (X02)	
89	12	2018/12/18	Follow spyglass, reserve for after global reset CNVI module lost issue	Add CNVI_EN# net connection to PCH side(GPP_H3), add RC868 PD(75K_0402_5%) for CNVI_EN#	0.3 (X02)	
90	52	2018/12/18	Follow spyglass, reserve for after global reset CNVI module lost issue	1.Add RZ827(0_0201_5%) connect to CNVI_EN# For reserve 2.Change net name from CNV_RF_RESET to CNV_DET#_EC	0.3 (X02)	
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